A Single Stage, Two Channel Ka-band to Digital, Therally Compensating Receiver for SWOT

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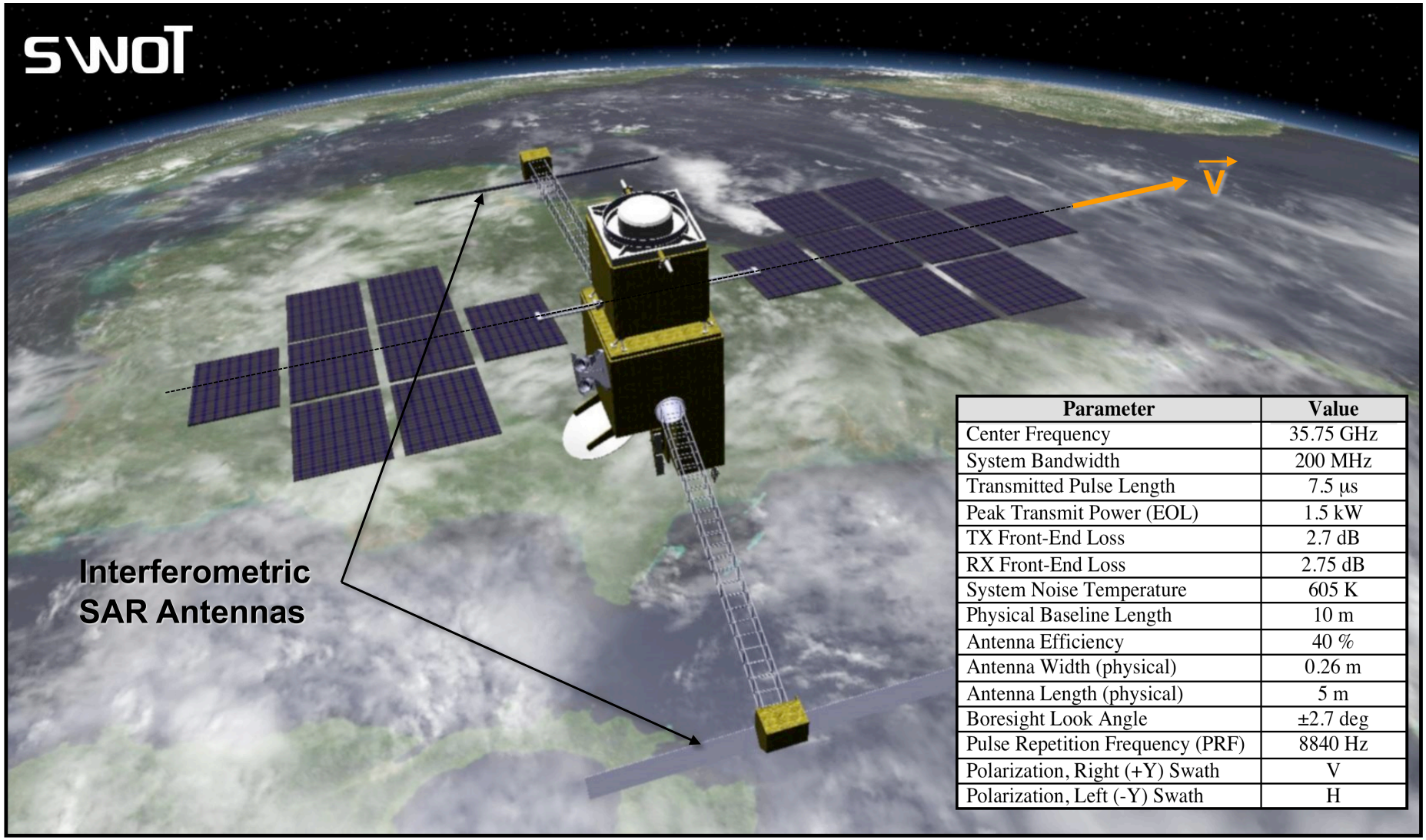
Talk Outline

- SWOT Mission & Project Outline
- Single-stage and two-stage downconversion
- Thermal Analysis of RF subsystem
- Space Qualifiable High-speed (2x3GSamp/sec ADC/FPGA Board)
- TRL Advancement

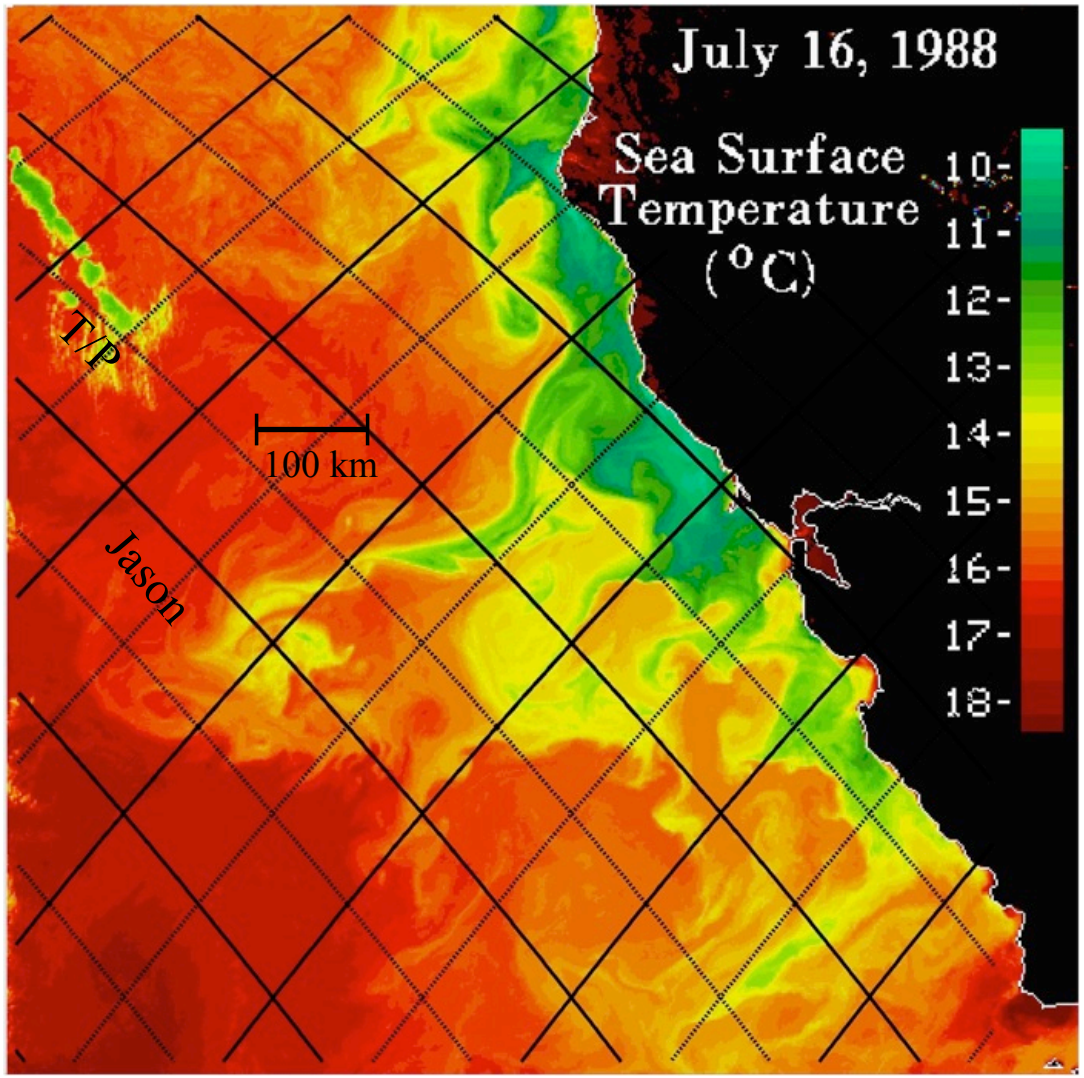
KaRIn Baseline Parameters

SWOT Downconverter



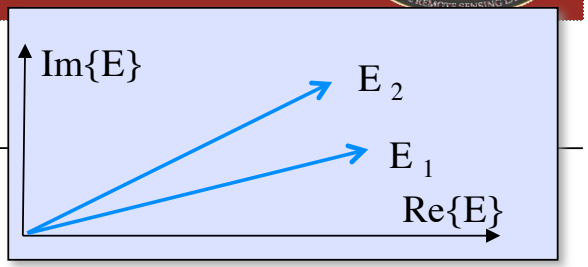
Parameter	Value
Center Frequency	35.75 GHz
System Bandwidth	200 MHz
Transmitted Pulse Length	7.5 μs
Peak Transmit Power (EOL)	1.5 kW
TX Front-End Loss	2.7 dB
RX Front-End Loss	2.75 dB
System Noise Temperature	605 K
Physical Baseline Length	10 m
Antenna Efficiency	40 %
Antenna Width (physical)	0.26 m
Antenna Length (physical)	5 m
Boresight Look Angle	±2.7 deg
Pulse Repetition Frequency (PRF)	8840 Hz
Polarization, Right (+Y) Swath	V
Polarization, Left (-Y) Swath	H

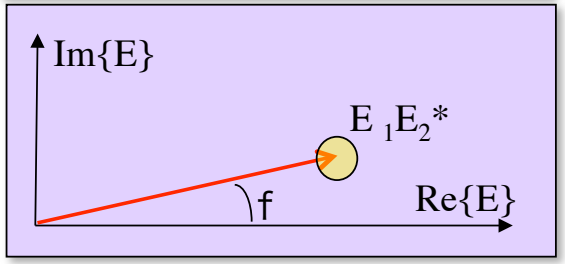
SWOT's Mapping Capability



- Submesoscale phenomena exhibit rich spatial patterns characteristic of turbulent mixing down to small scales
- **SWOT driving requirement:** resolve submesoscale phenomena in space and height
- Spatial scales where SSH is diagnostic of circulation: 10km-20km
- Height accuracies characteristic of those scales: 1cm @ 1km white noise levels
- For submesoscales, noise at high-frequencies has a higher impact than noise at low frequencies

Cross-Track Interferometry

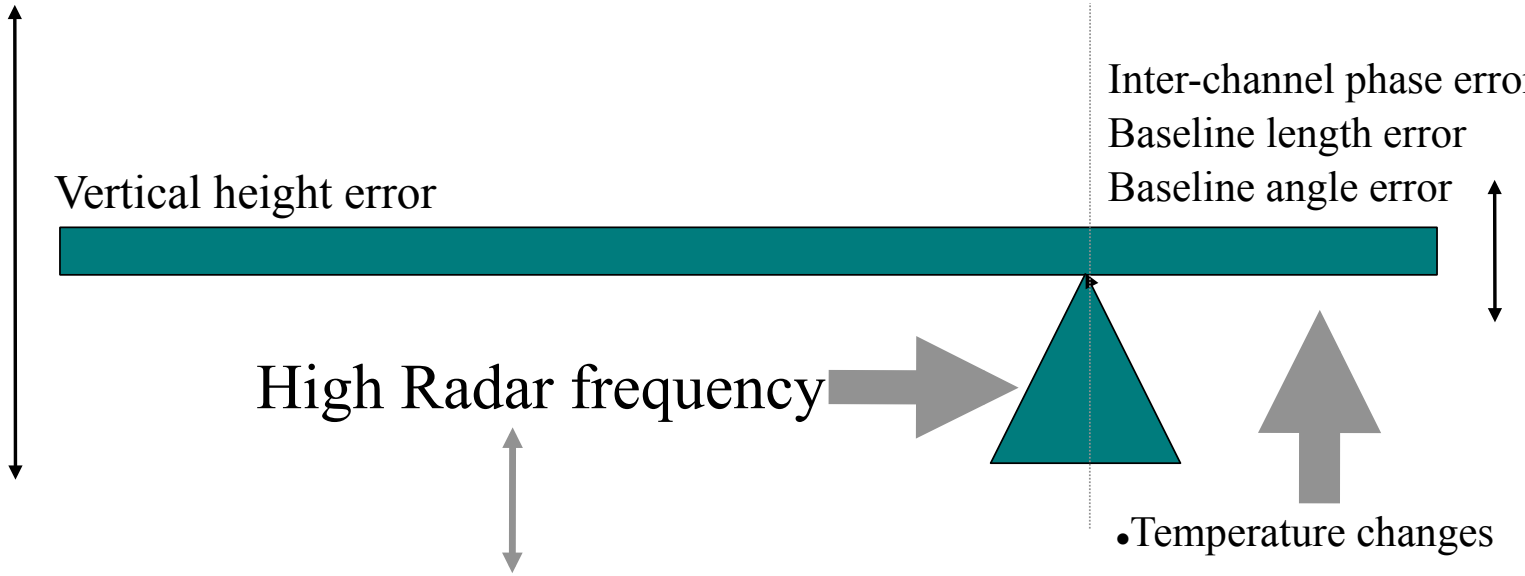




$$\theta = \sin^{-1}\left(\frac{\lambda\phi}{a2\pi B}\right)$$

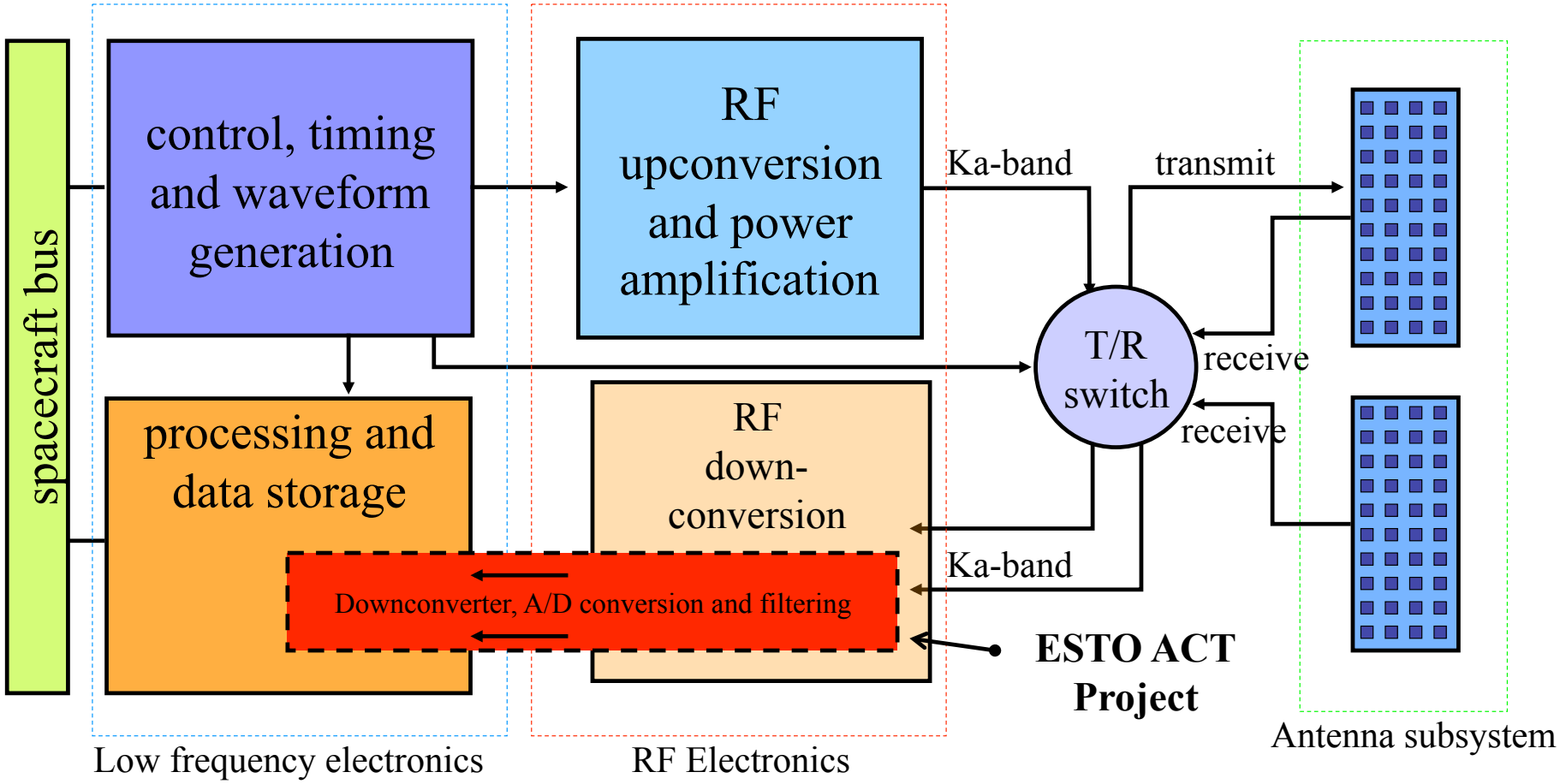
$$z = H - \rho\cos\left(\xi - \sin^{-1}\left(\frac{\lambda\phi}{a2\pi B}\right)\right)$$

Engineering Challenge

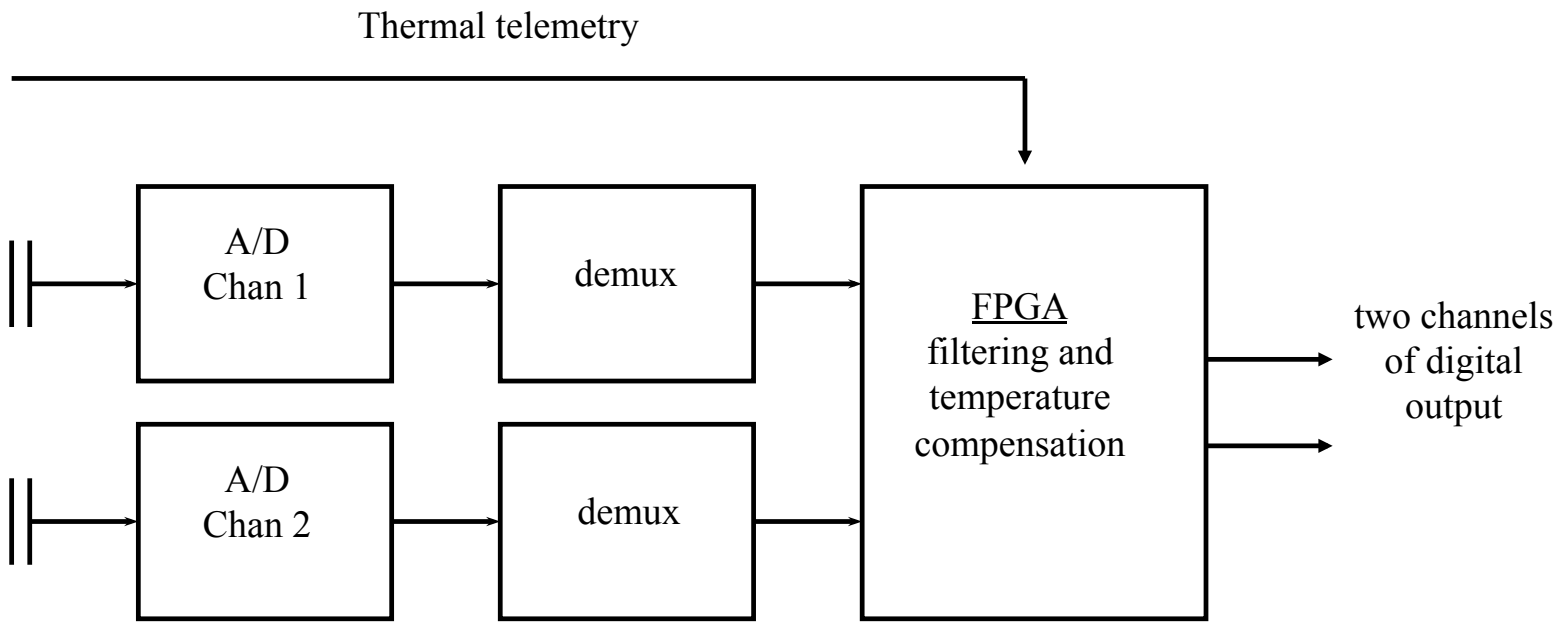


- Temperature changes
- Nonlinear operations during downconversion
- Mechanical vibrations
- External interference

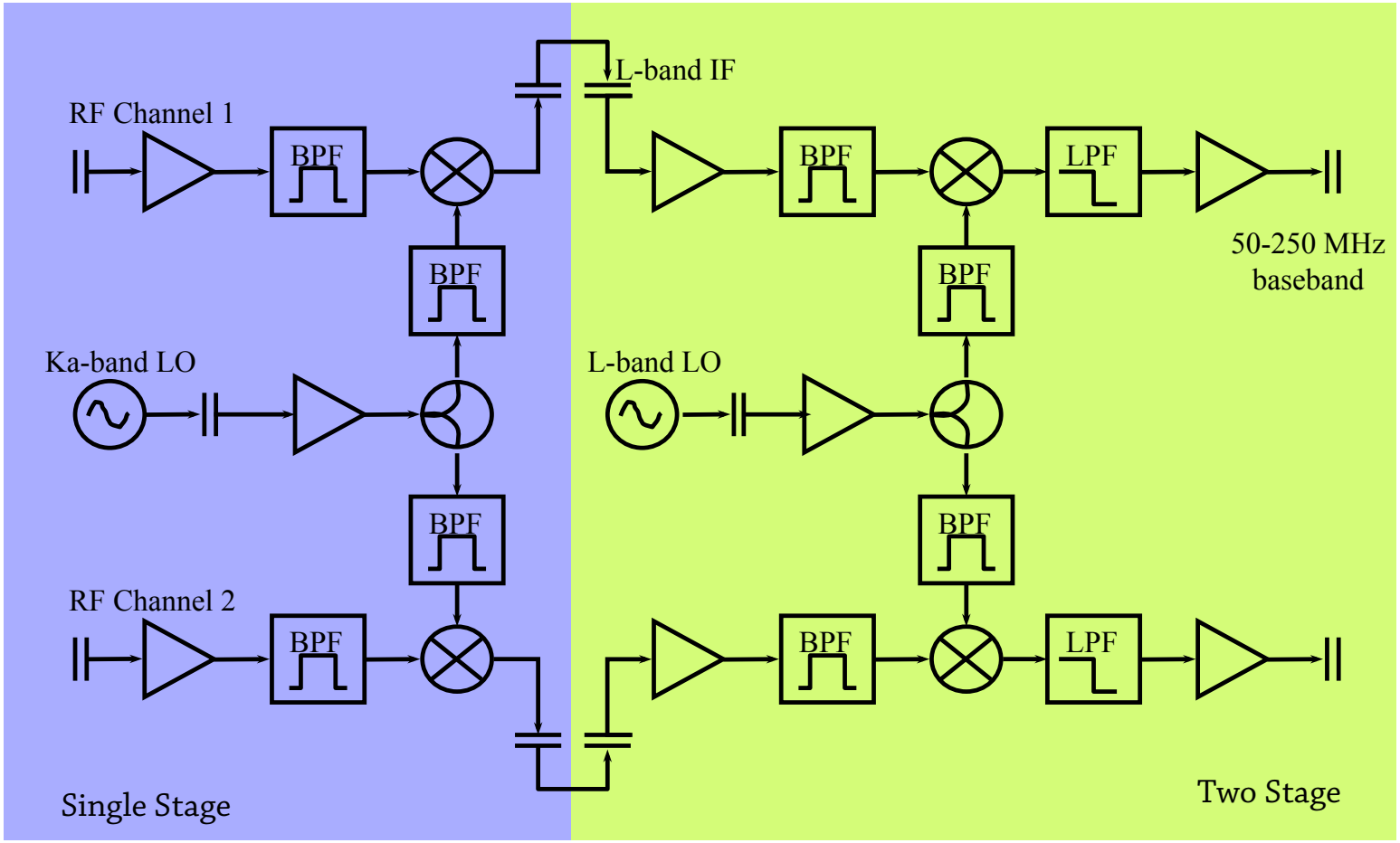
Spacecraft block diagram



Thermal Telemetry combined with Science Data



Single- and Double-stage downconversion



One-Stage Down Conversion vs. Two-Stages

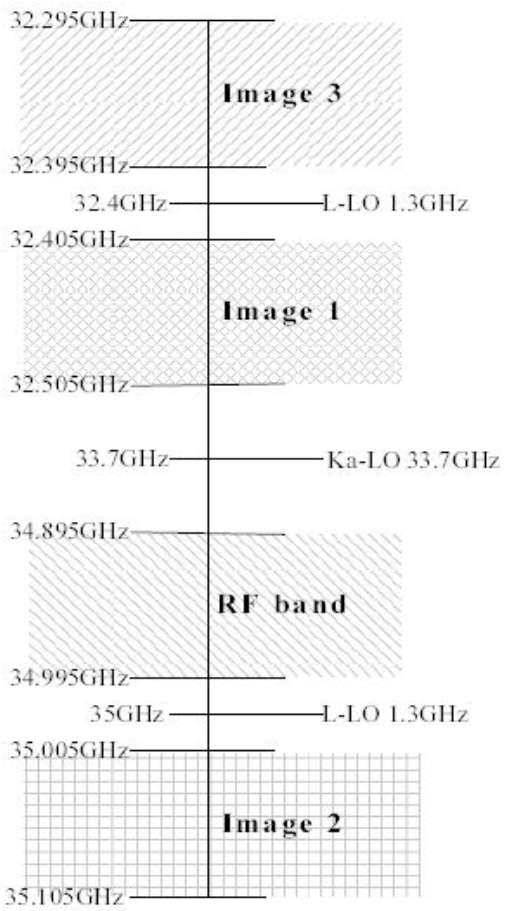
Two architectures are being explored for converting the high frequency (Ka-band) science data into digital signals.

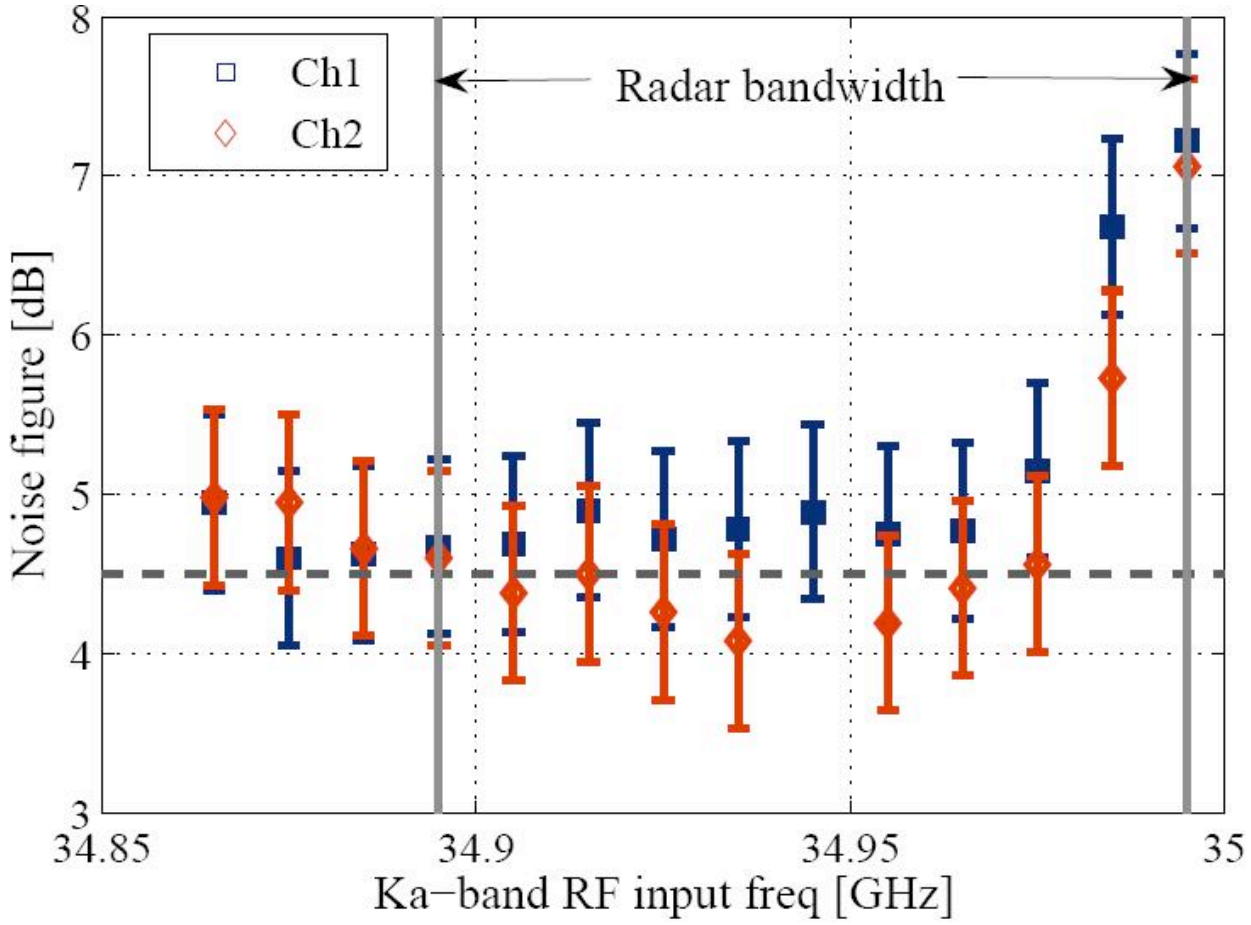
One architecture is to perform a single-stage downconversion from Ka-band to L-band, and then to sample this L-band signal using a high speed A/D converter (e.g. Analog Devices 1520, 3GS/sec). In this implementation, filtering can be done either digitally (via an on-board FPGA) or in analog, and has the advantage of flexibility and simplicity.

Another architecture uses two stages of downconversion, one to a high L- or S-band intermediate frequency (IF), and then a second stage of downconversion to baseband. This has the advantage of being able to run the A/D converter at a lower frequency and perform the noise bandwidth and alias rejection filtering in analog, thus having the potential of power savings.

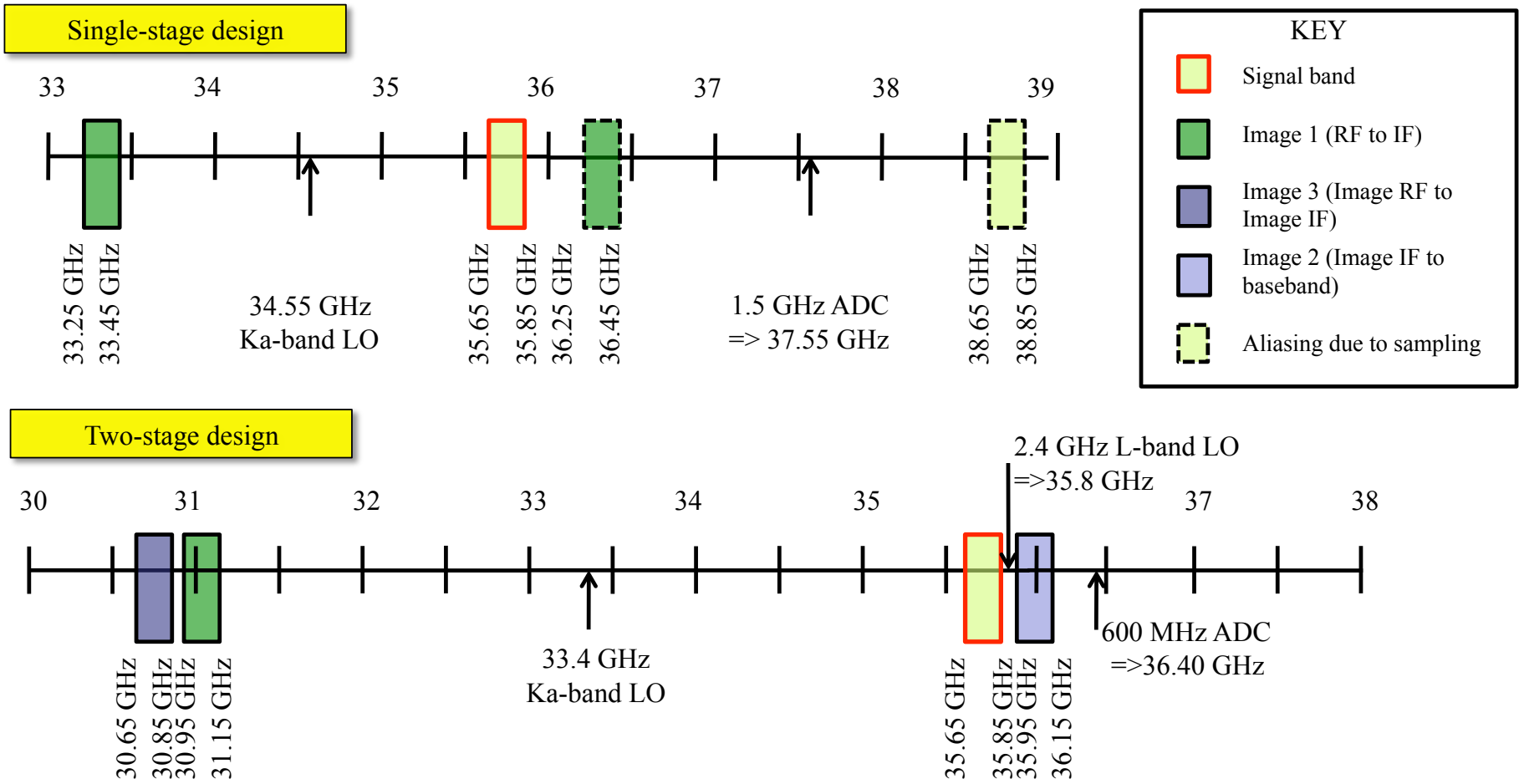
A third architecture that will not be implemented, is that of undersampling the single-stage downconverted signal. This is because the process of undersampling substantially increases the system phase noise. Phase noise is an error source that the two-channel interferometric downconverter is particularly sensitive to.

Bandpass Characteristics for a Two-stage downconverter



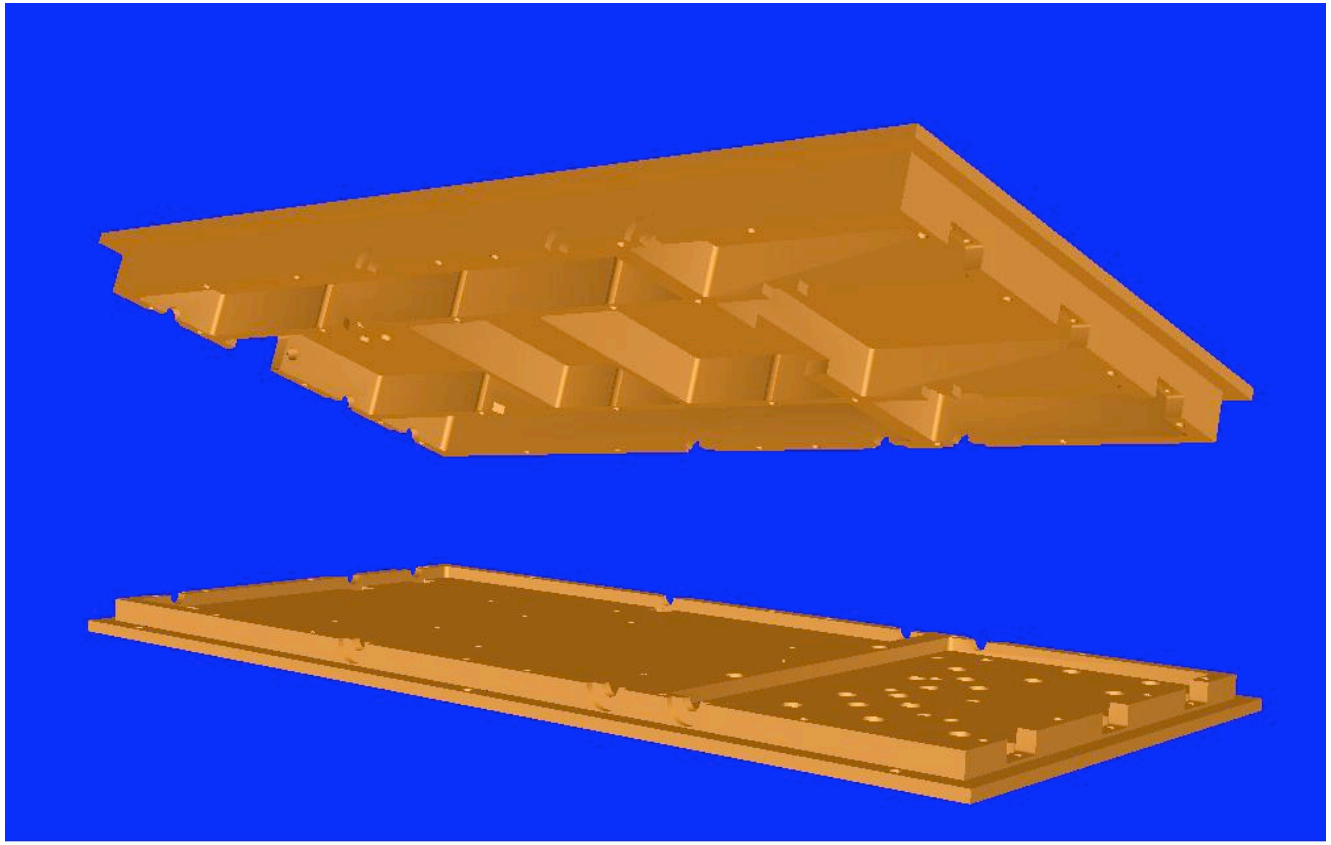


Images from Downconversion and Sampling

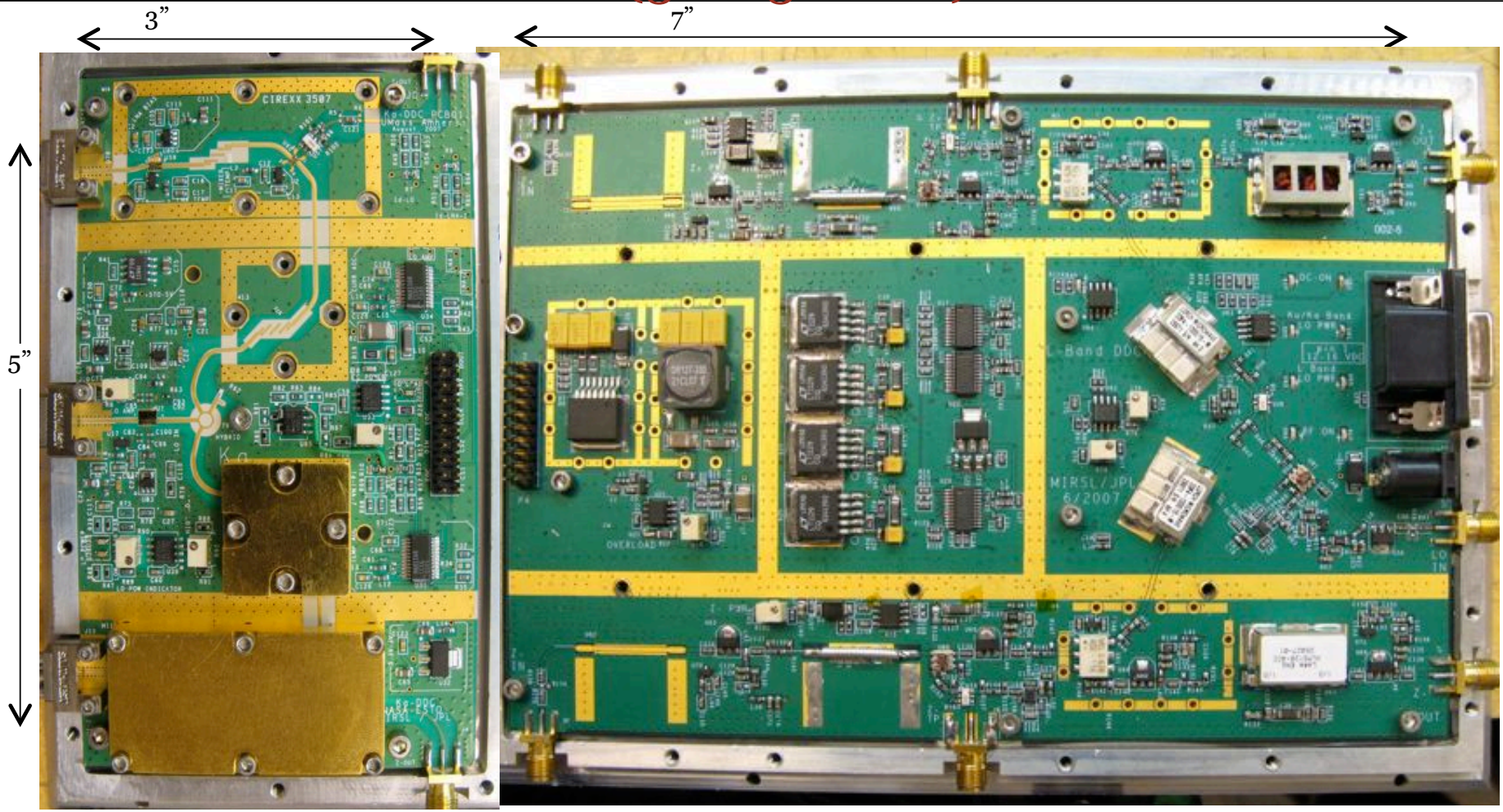


Combined system Ka-band Mechanical Housing

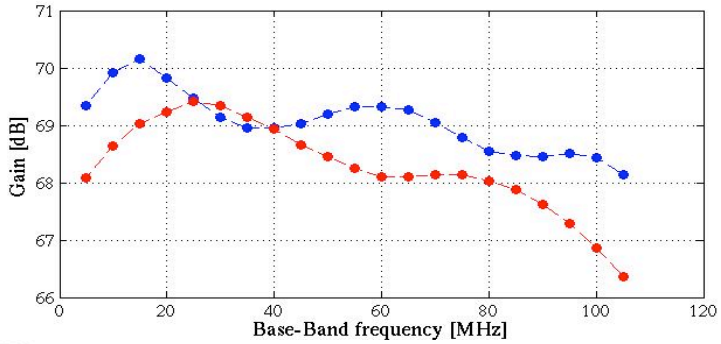
Additional cavity walls carved into housing to improve isolation

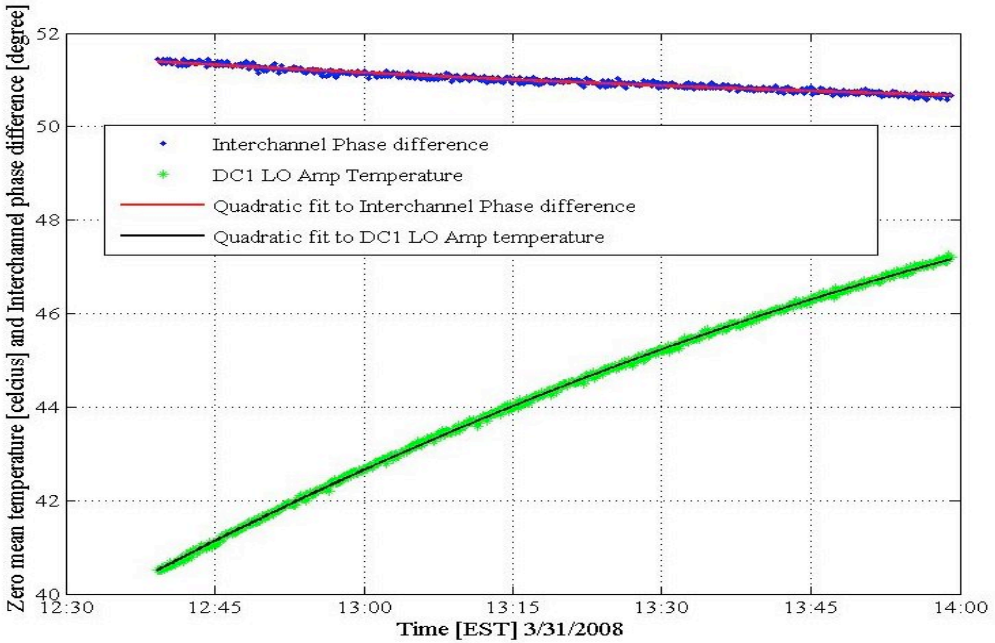


The Ka-band to UHF (5-105 MHz) DDC



Basic Performance Characteristics of Current System





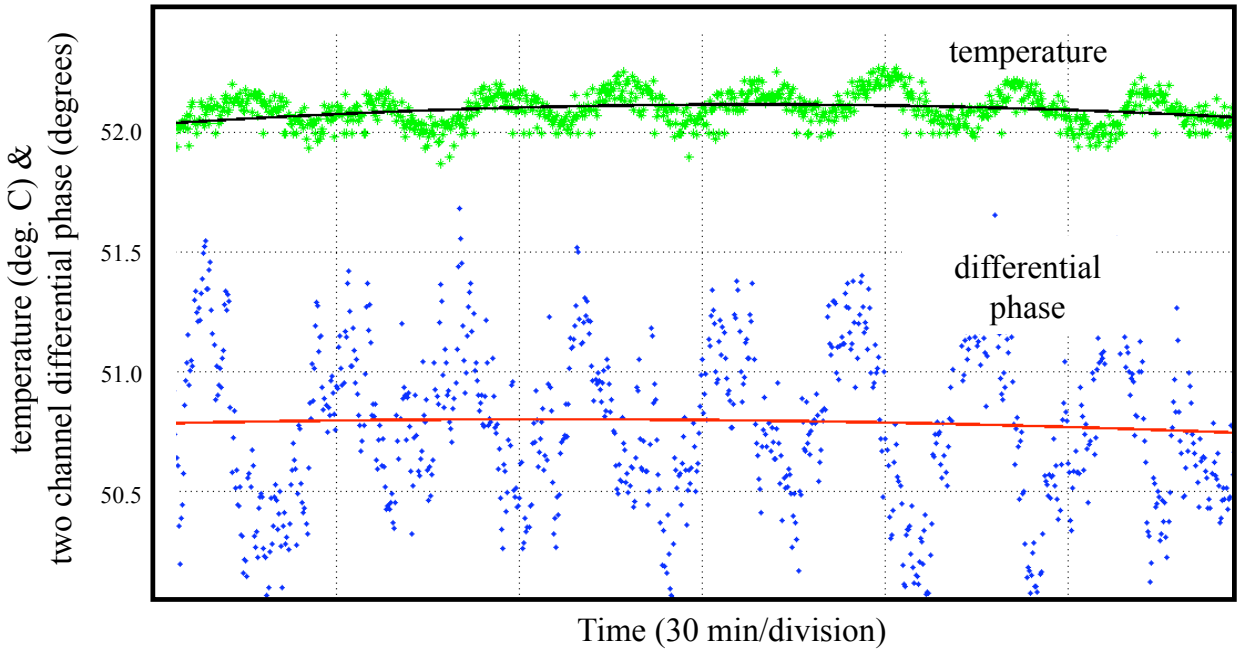
Supply = 14.5 V, 830 mA
Power = 12W

Two-Channel Gain Balance=1.5dB
Nominal Gain = 70 dB
P1dB=19dBm
Noise figure=3.5dB
Input Return Loss ~ 11 dB
Two-channel isoloation = 66 dB

Inter-channel phase difference stability (Standard Deviation) = 0.213°

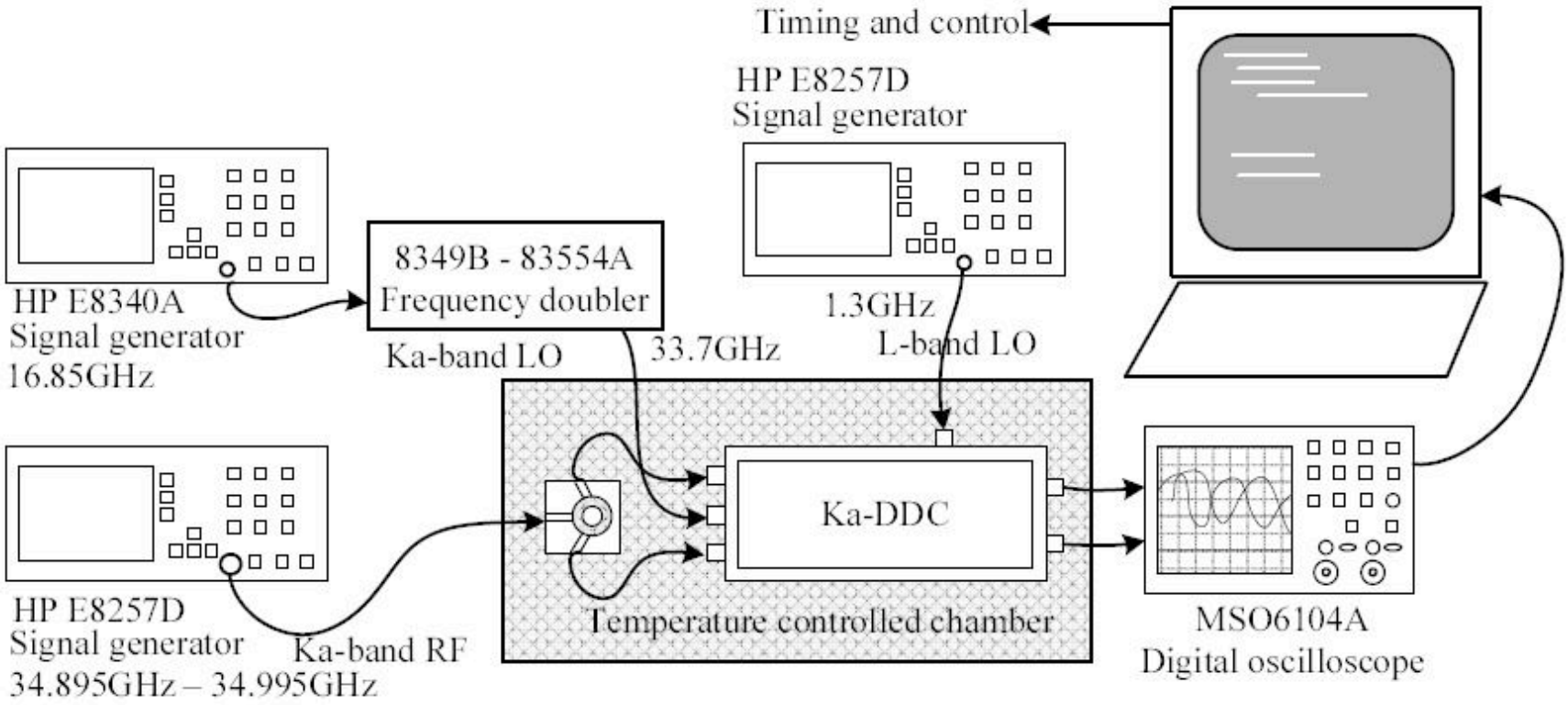
Phase standard deviation from best quadratic fit = 0.04° (0.05 ° rqmt.)

Temperature dependence of differential phase



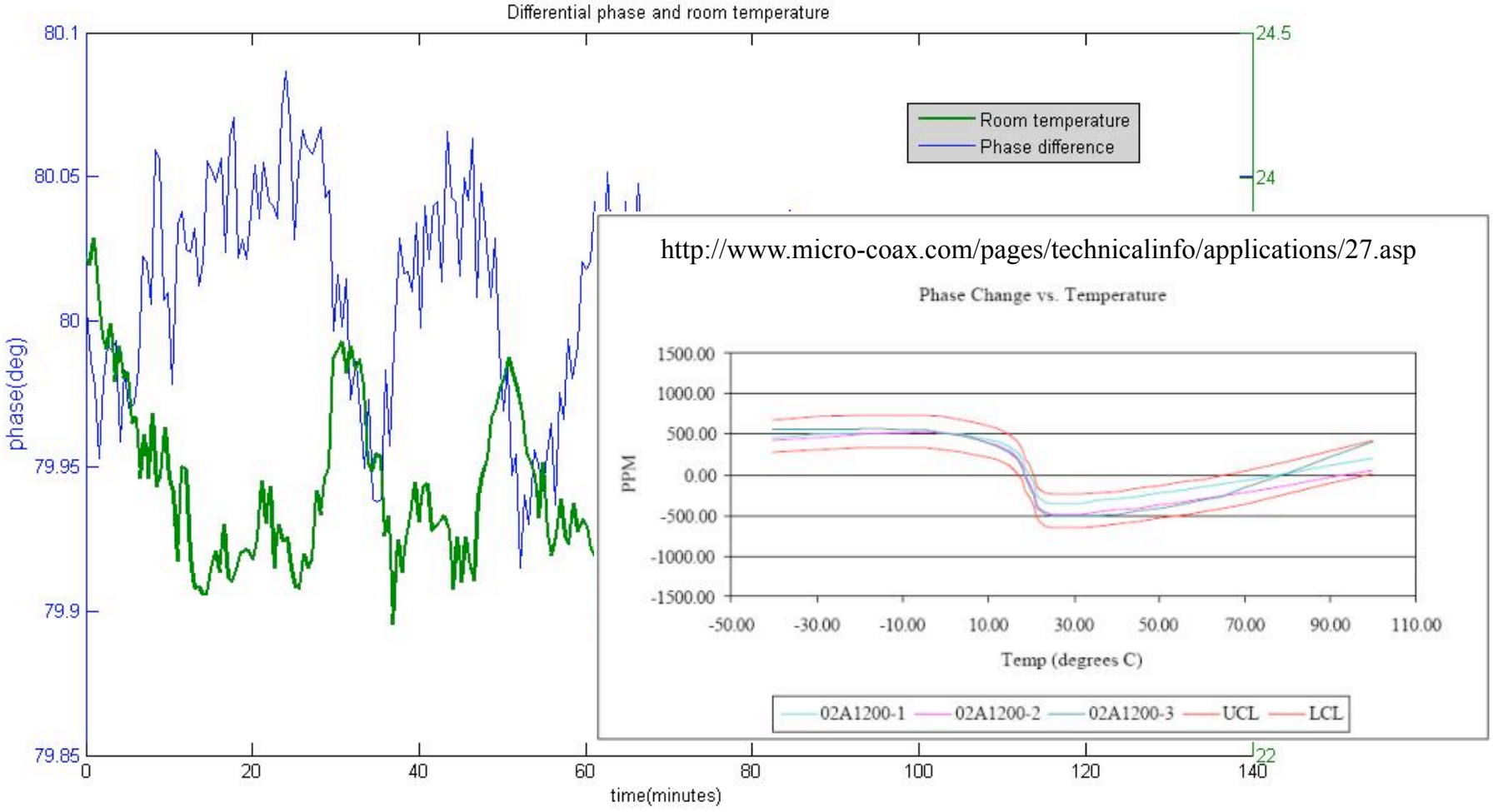
- Concurrent measurements of temperature and differentail phase showed a strong dependence of phase on temperature.
- Temperature fluctuations due to the ambient enviroment. Measurements in a closed environment were much more stable
- Solid lines in the plot indicate a 3rd order polynomial fit to the data.

Thermal characterization

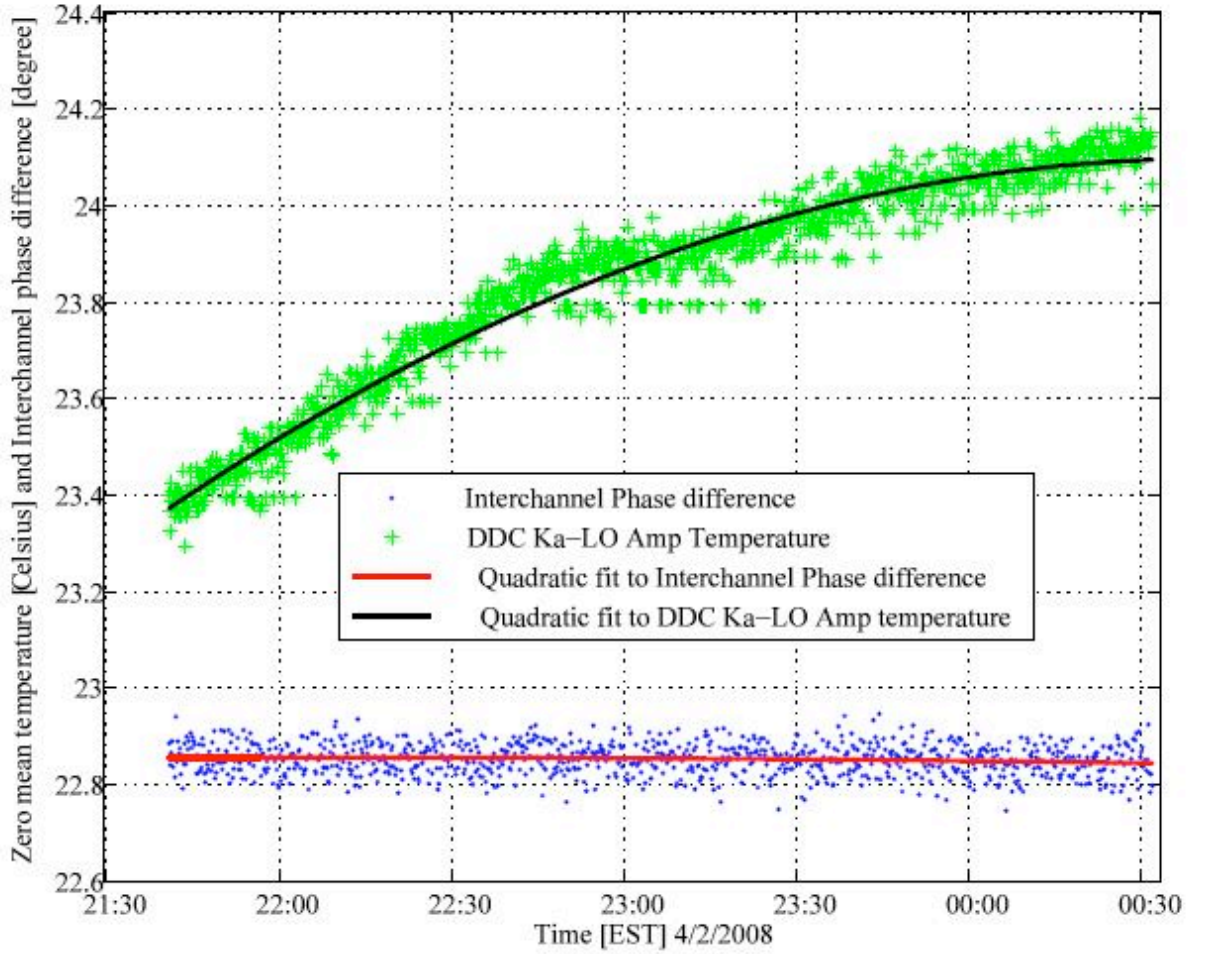


Siqueira, Ahmed, Wirth, and Bachmann, "Variable Precision Two-Channel Phase, Amplitude and Timing Measurements for Radar Interferometry and Polarimetry," IEEE Trans. Micrw. Theor. Tech., 55(10), 2248-2256, 2007.

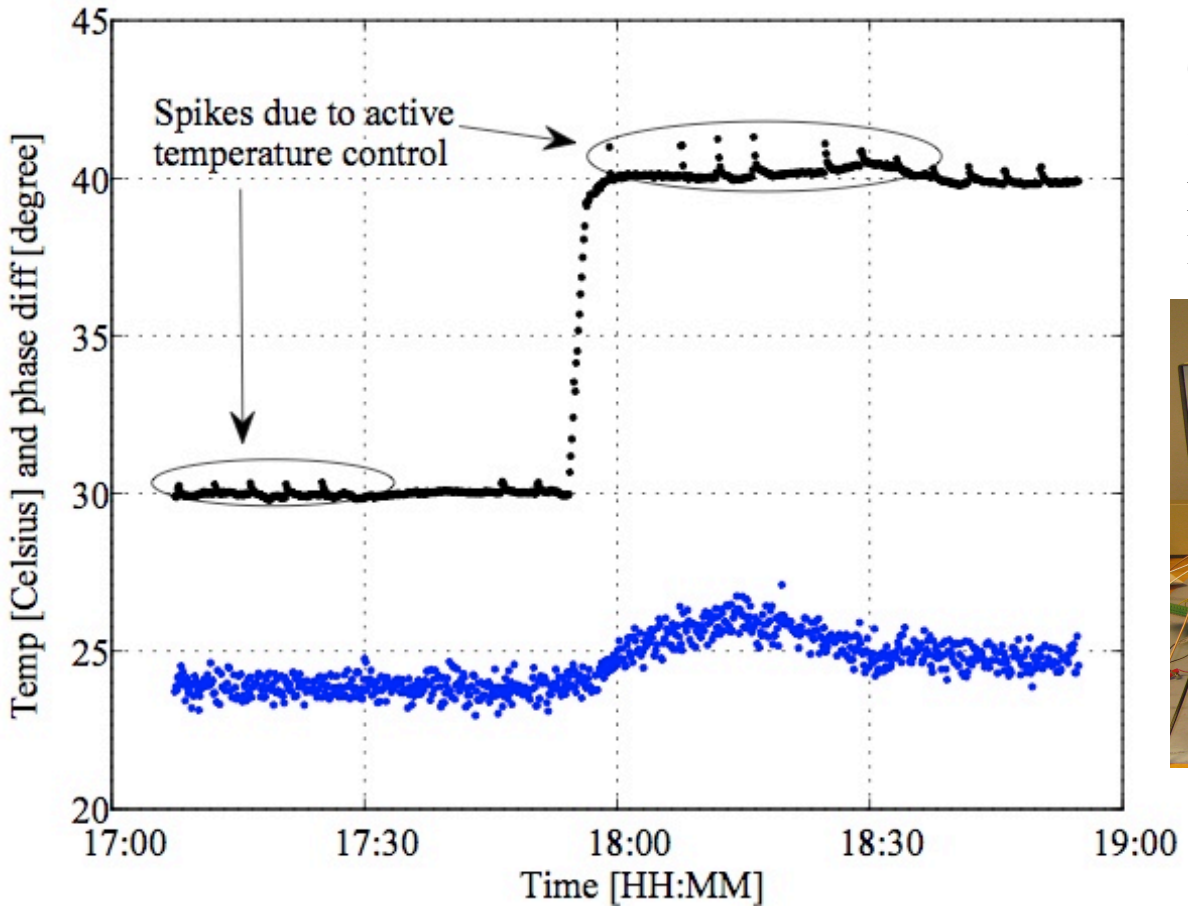
A simple demo (100 MHz, 8.7m cable length, -> 8.3mm/°C change)



Temperature and Phase Fluctuations in a Protected Environment

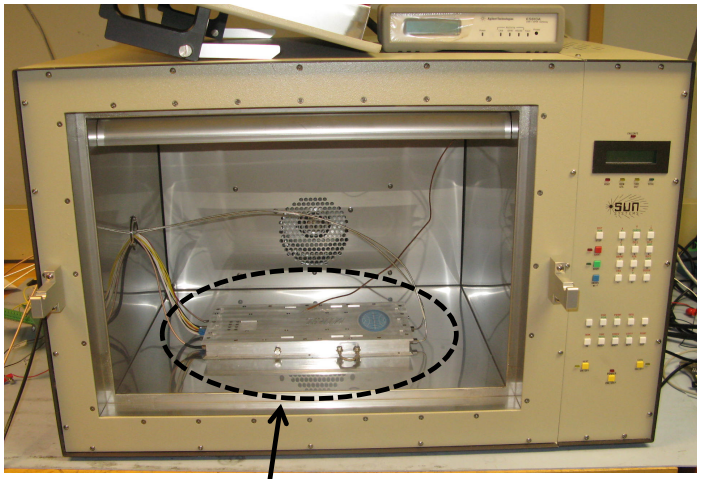


Thermal Testing and Characterization is a tricky affair

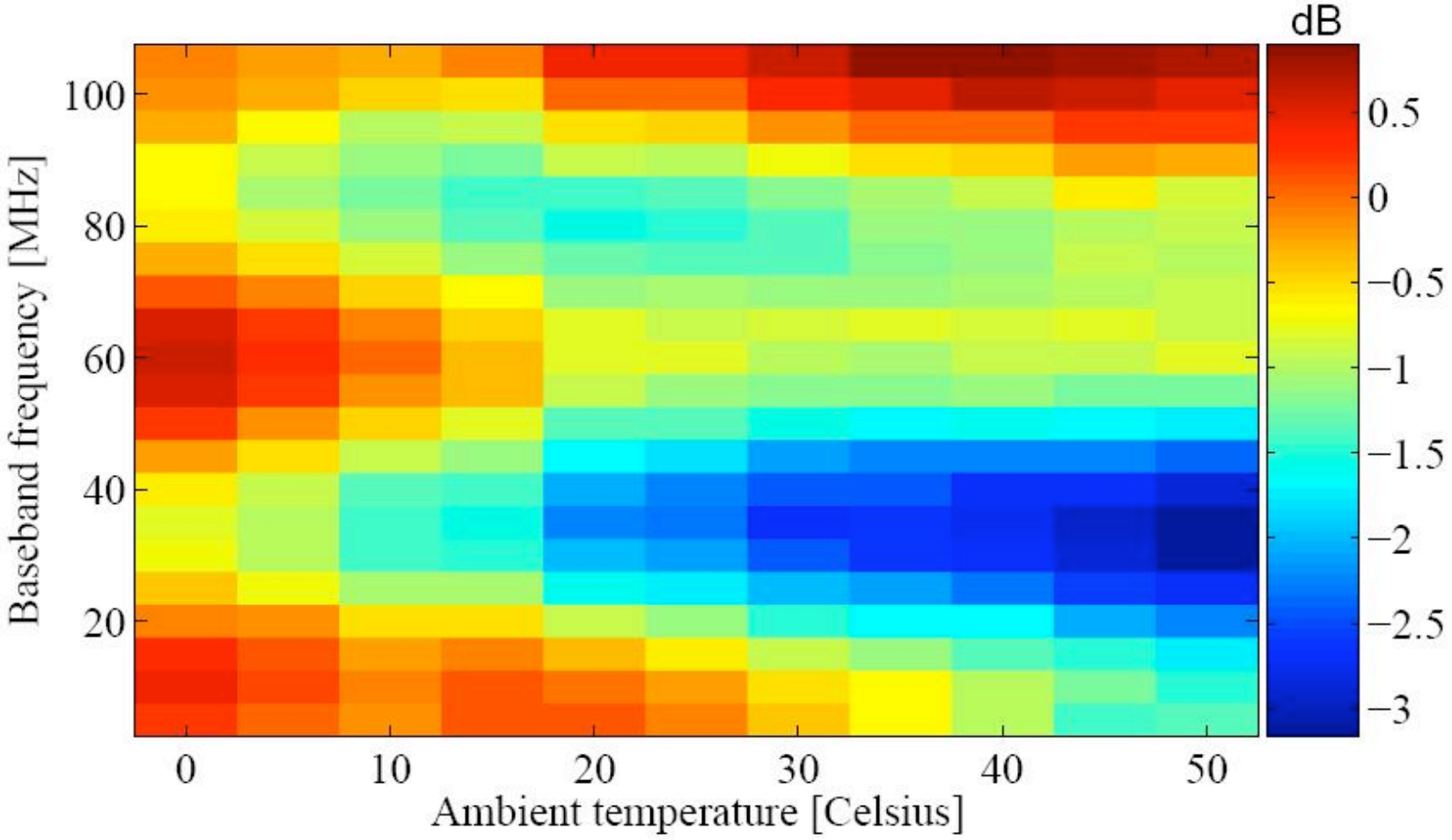


0.25°C/second, 15°C/min; -100°C to 300°C temperature range

Remote operation via serial port or IEEE-488 bus



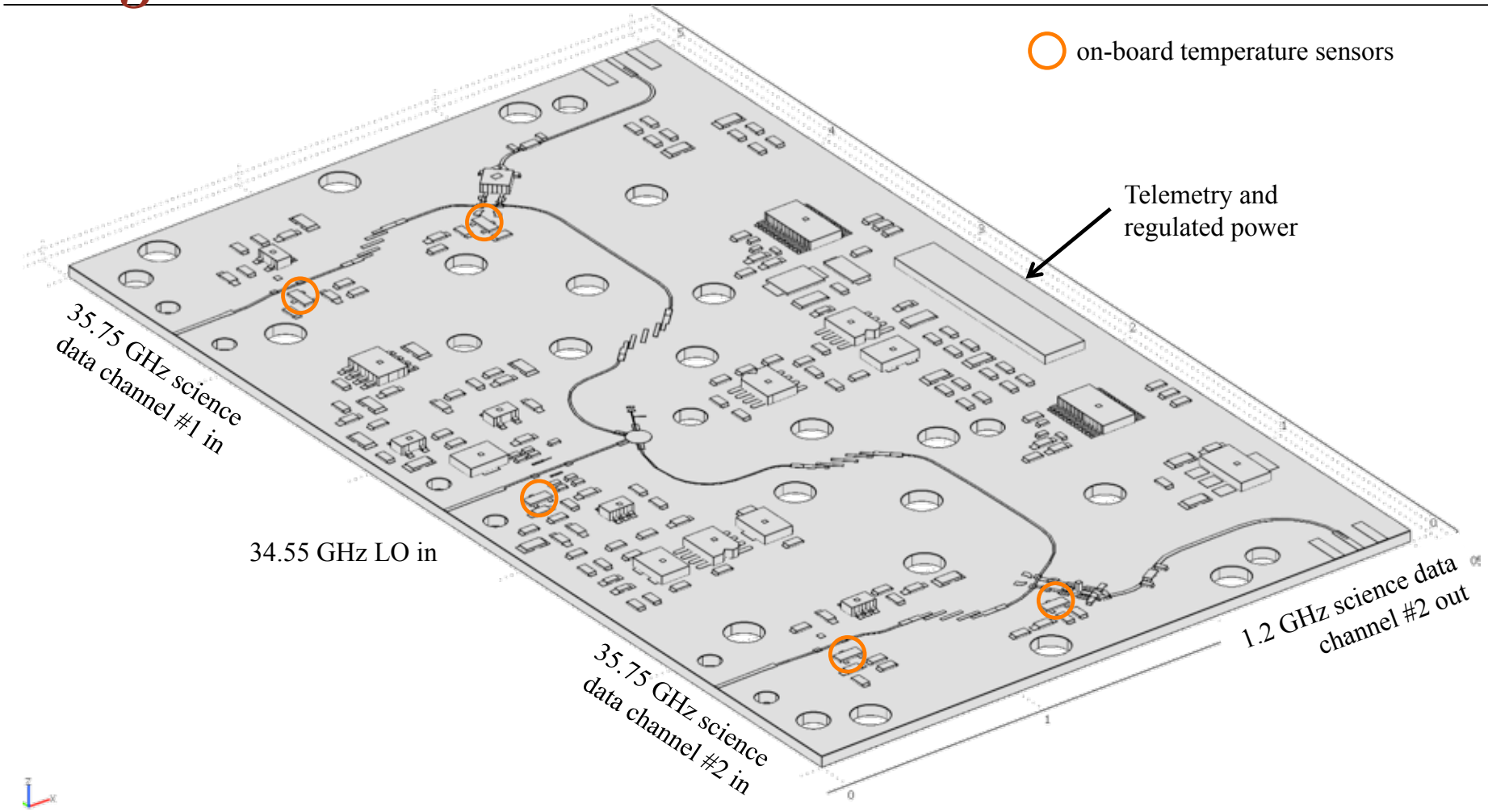
Gain variation over temperature



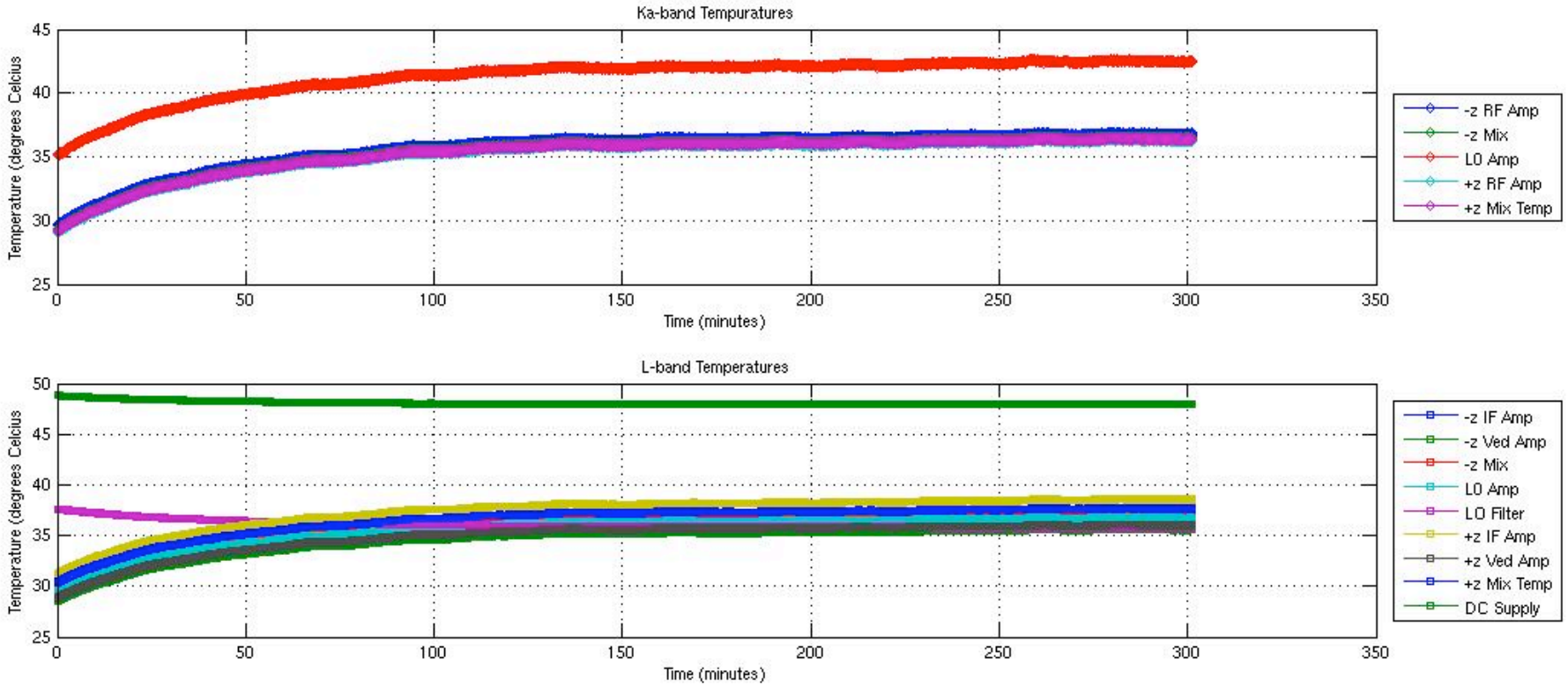
Thermal Analysis

- 35 GHz signals have a wavelength of 8.4 mm.
- Changes in the physical path length due to thermal expansion/contraction, will cause changes in the signal phase.
- A one degree phase change is equivalent to 23 mm of electrical path length change. Integrated over 5 cm of total path length, this is equivalent to a 0.05% expansion coefficient, or 5 parts in 10,000.
- Thermal imbalances between the two interferometric paths will thus induce a temperature dependent phase error.
- We are measuring temperature "on-board" so that this phase error may be monitored and corrected in the digital stage.
- Point measures of temperature are unlikely to be sufficient to characterize the phase error, as they do not take into account temperature distributions or the thermal inertia of the chassis
- Thermal modeling will help understand the source of thermal imbalance as it is distributed troughout the system

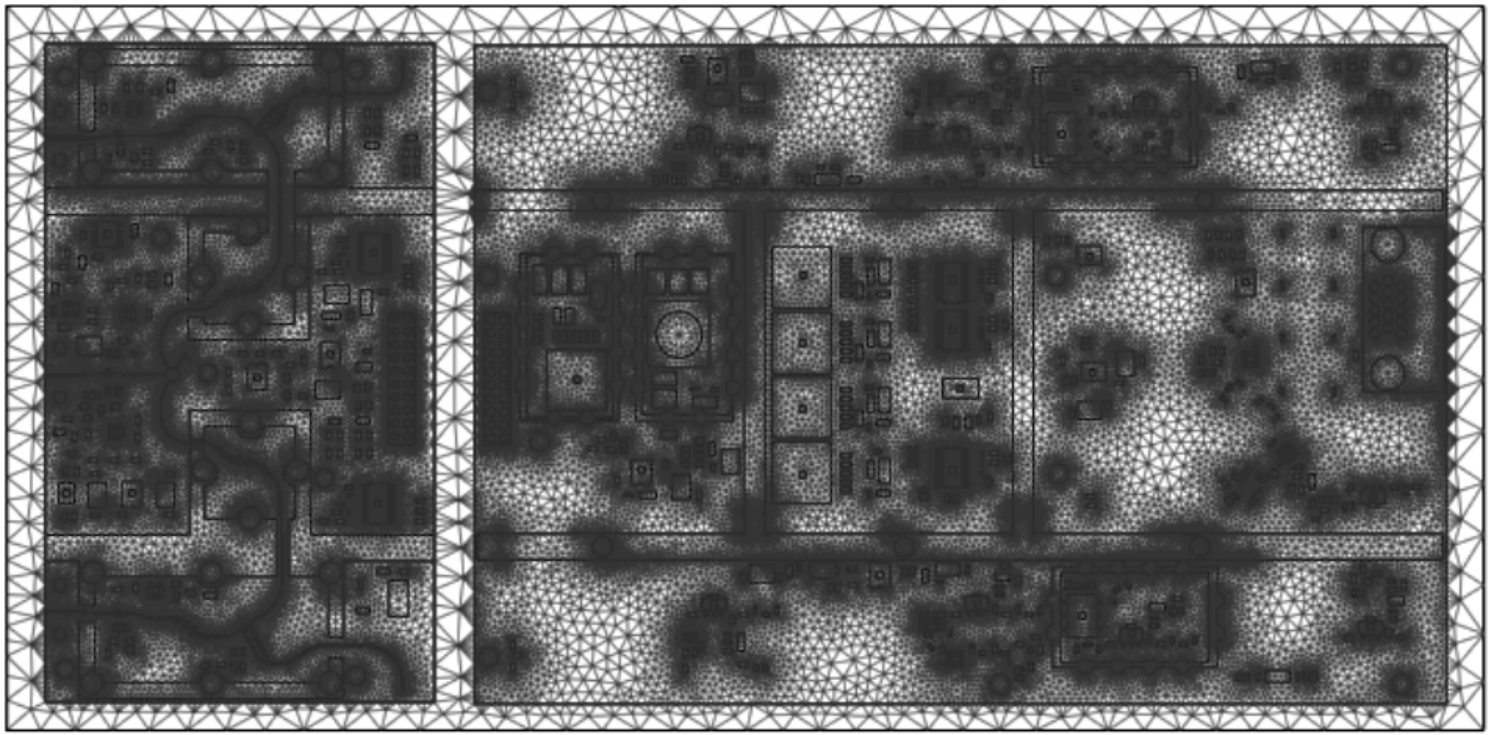
A 3D-relief of the Ka-band board



On-board Thermal Measurements



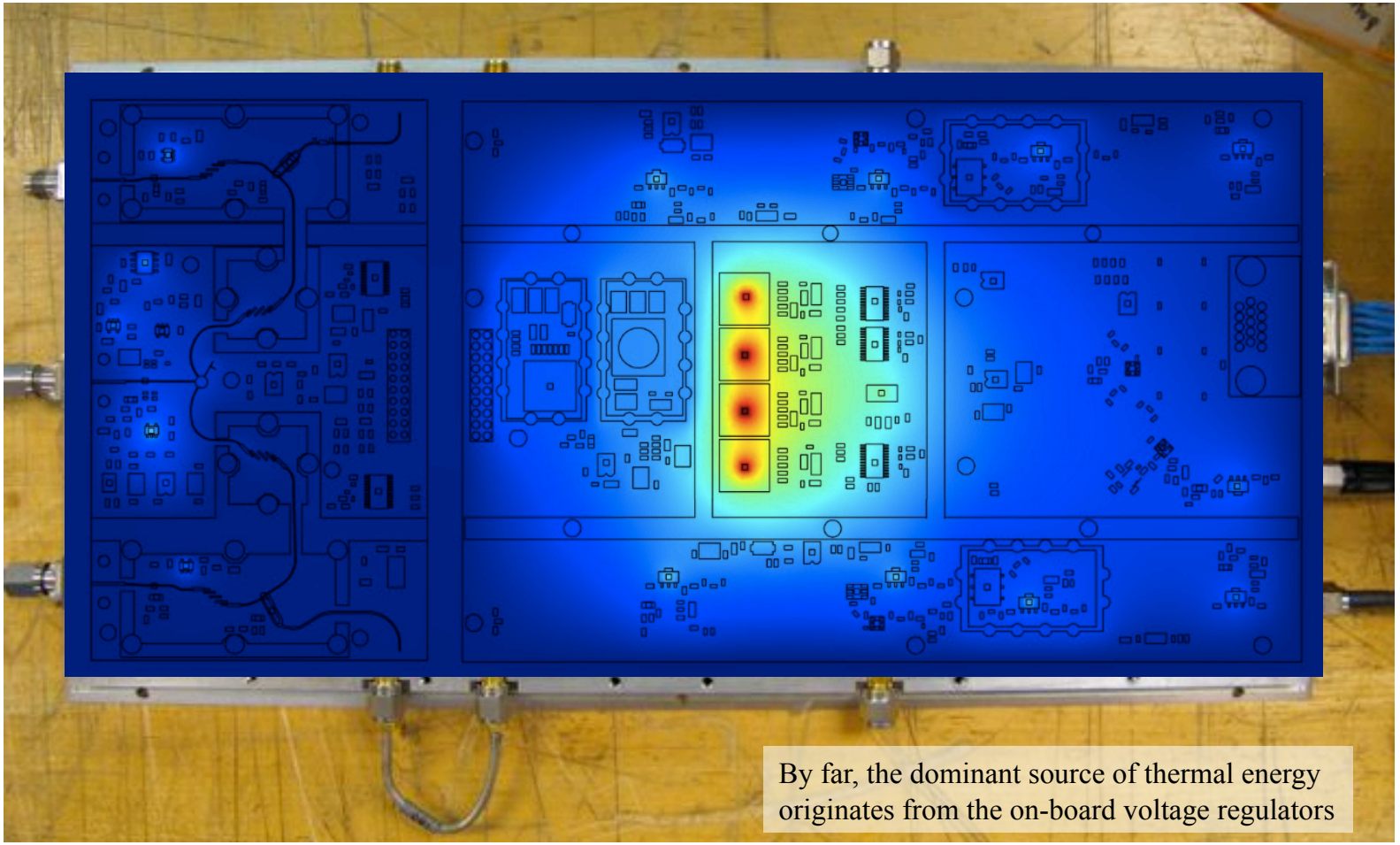
Thermal Analysis: FEM Mesh



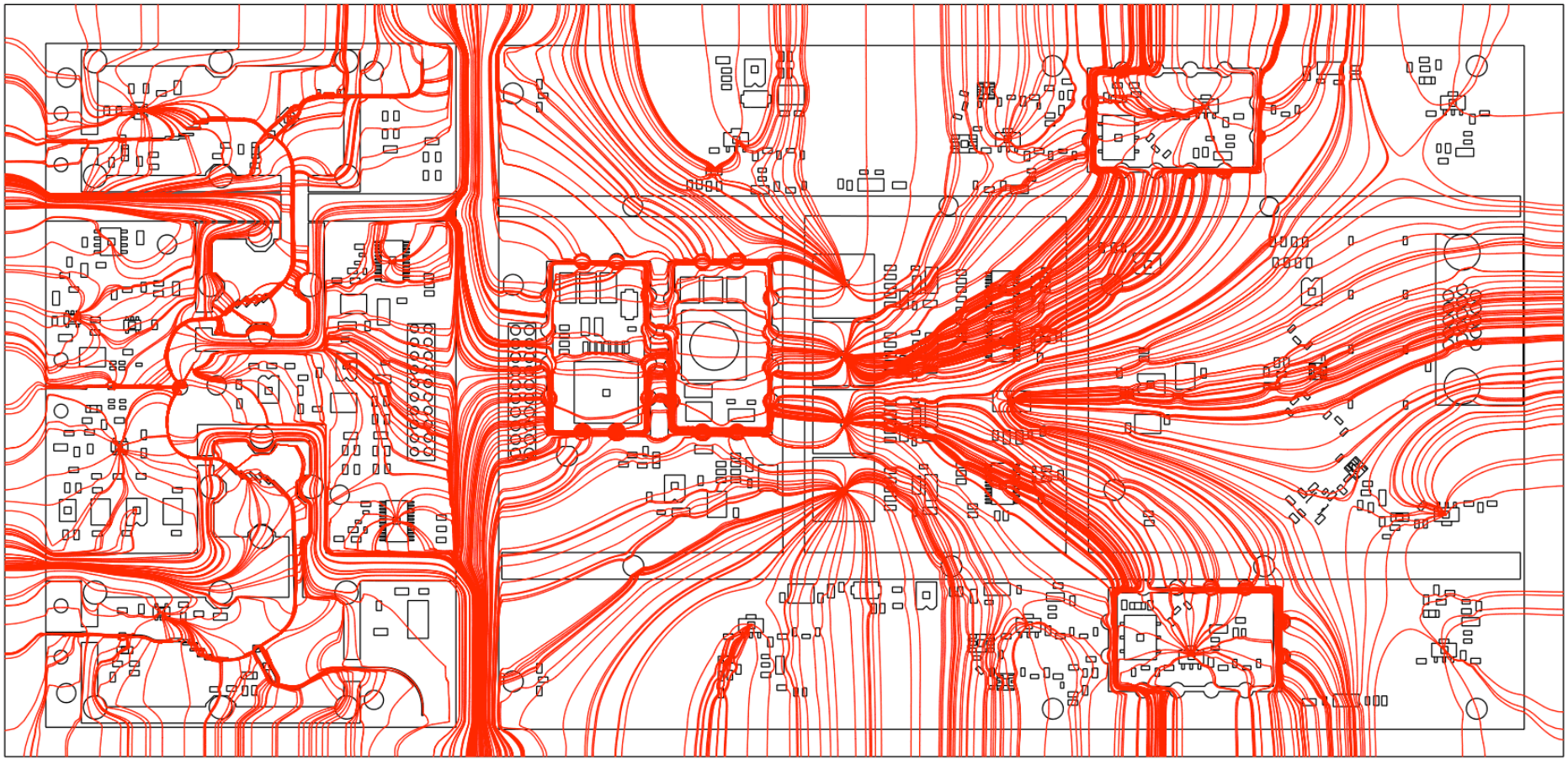
A commercial software package (COMSOL) is used to peform a thermal analysis on the existing downconverter board. The first step in the analysis is to generate a mesh for exercising the heat equation using the finite element method (FEM). For this analysis, radiative boundary conditions were used outside of the chassis, which was kept at room temperature.

Thermal Analysis Results*

* The association between color and temperature is still being calibrated.



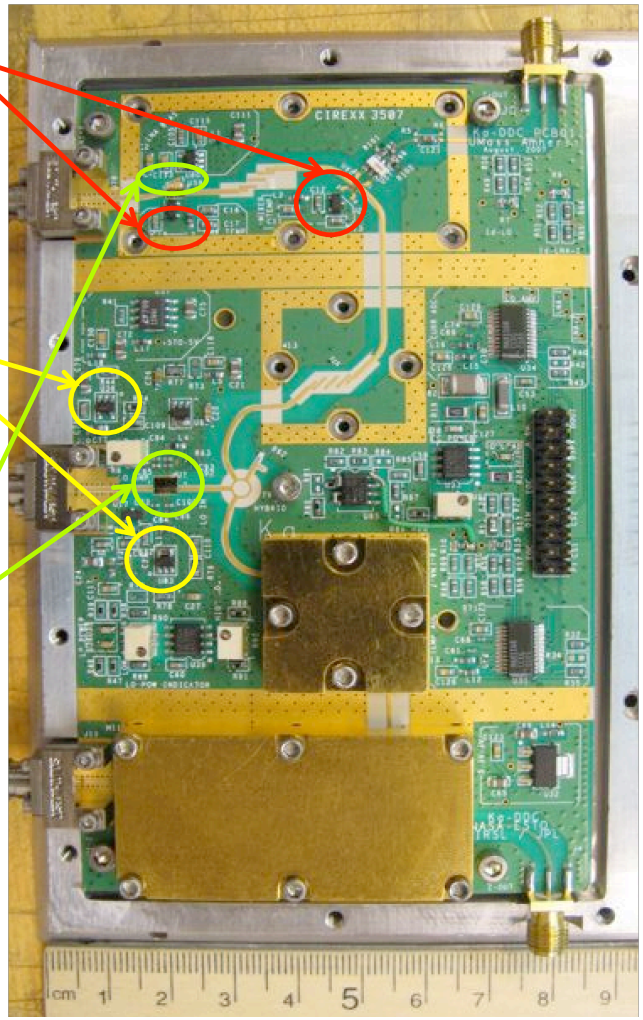
Heat Flow in the Two-stage Downconverter



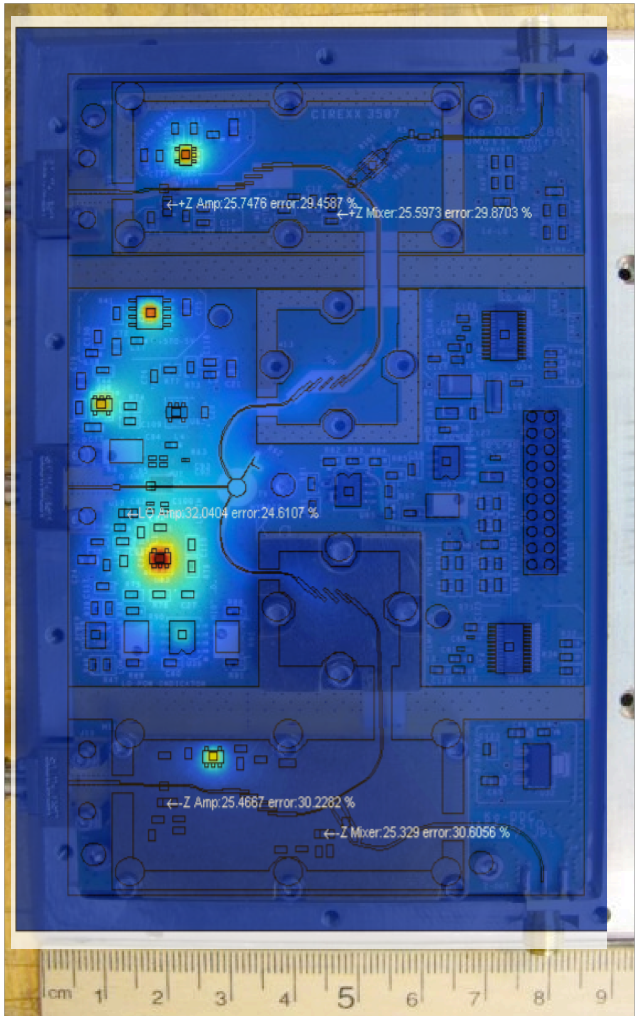
Determining the temperature gradient yields flux lines which describe the flow of thermal energy in the system. It is evident from the diagram (and practical knowledge) that the majority of heat is transferred through the metal chassis and PCB surfaces

Thermal Analysis of the Ka-band to L-band DC

Ka-band board

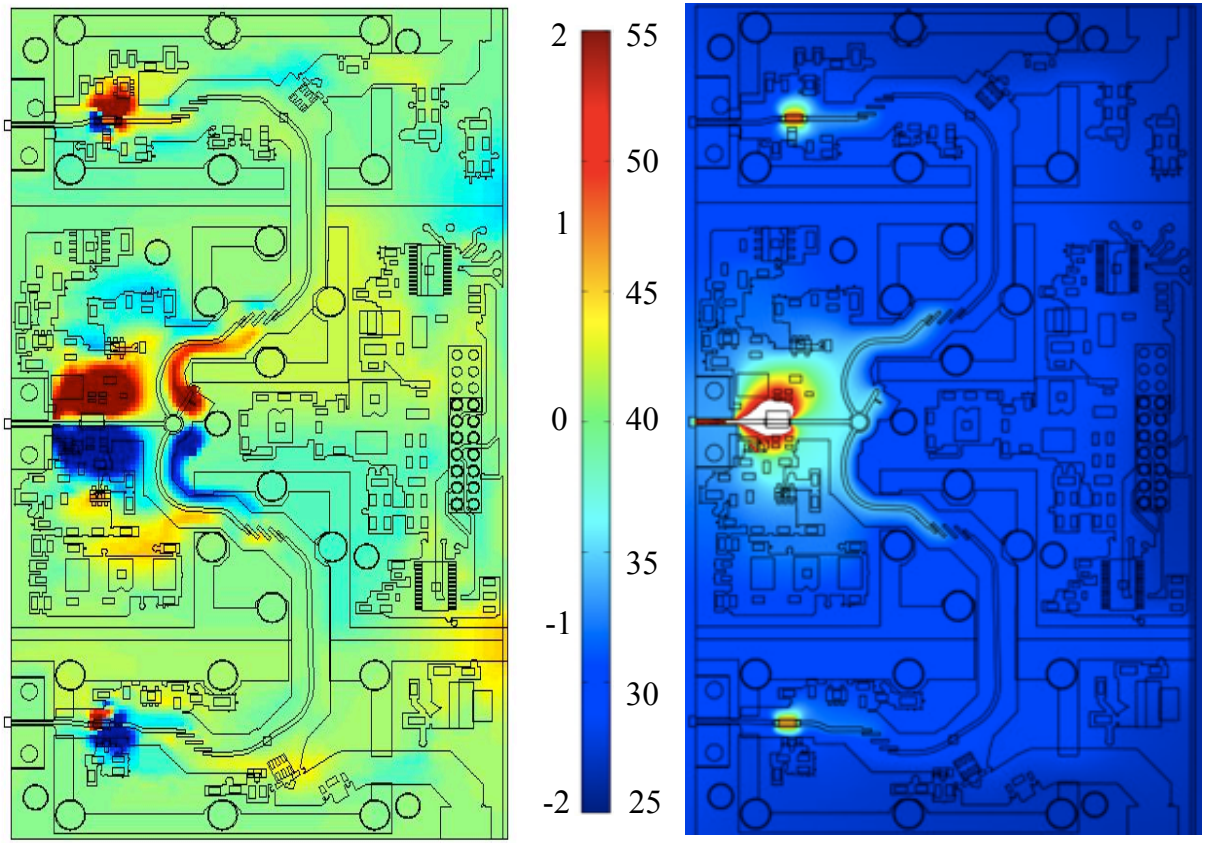


Thermal Analysis



Thermal analysis from COMSOL. Indicated on the plot are also point temperature measurements

Modeled Thermal Imbalance

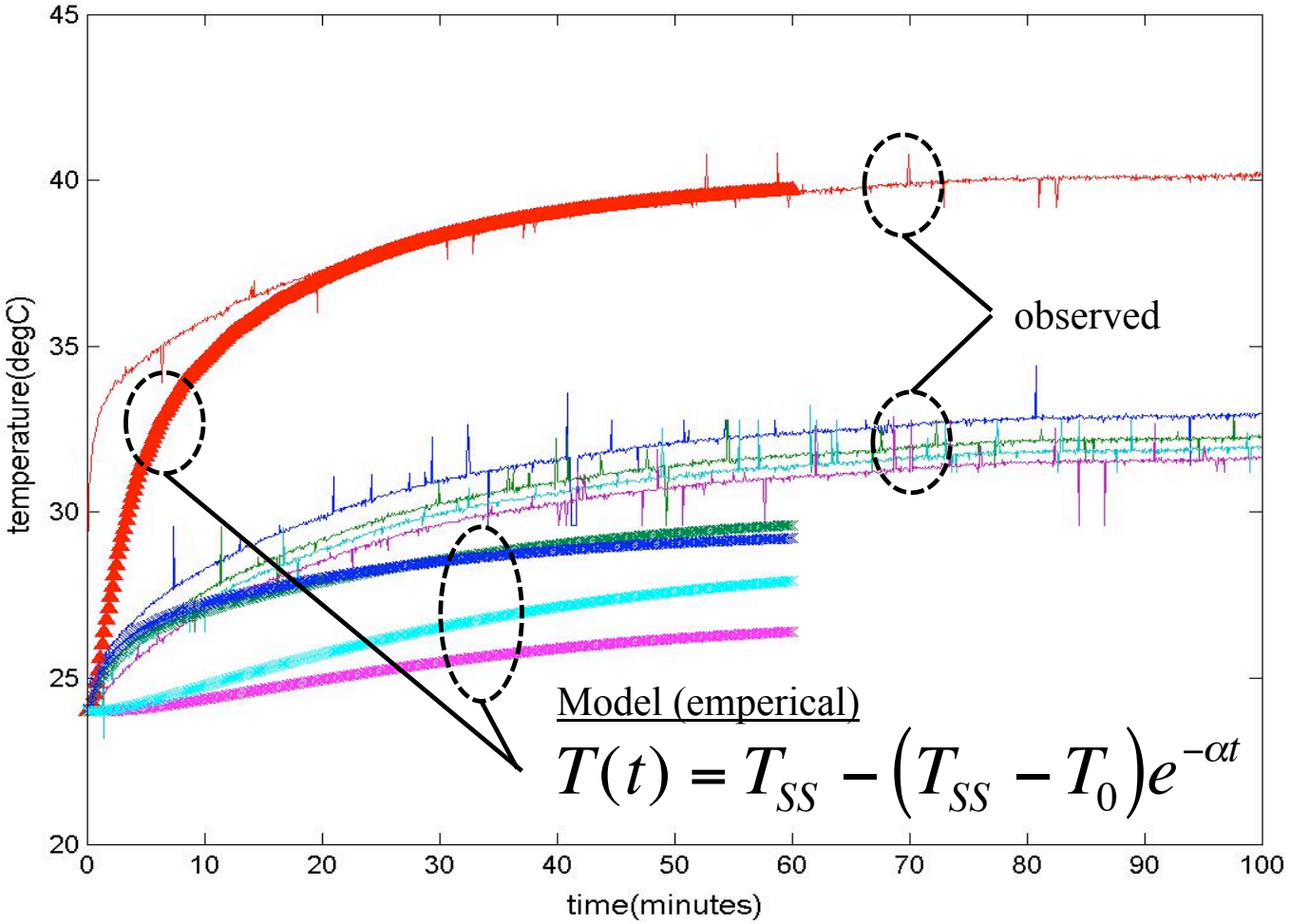


Temperature imbalance (°C)

Temperature (°C)

- Thermal assymetry in the downconverter design will lead to an assymetry in the electrical path length
- While this is not a bad thing in of itself, in a dynamic temperature environment, it will create a bias in the phase measurements, and hence the inferred height

Dynamic Modeling of Temperature



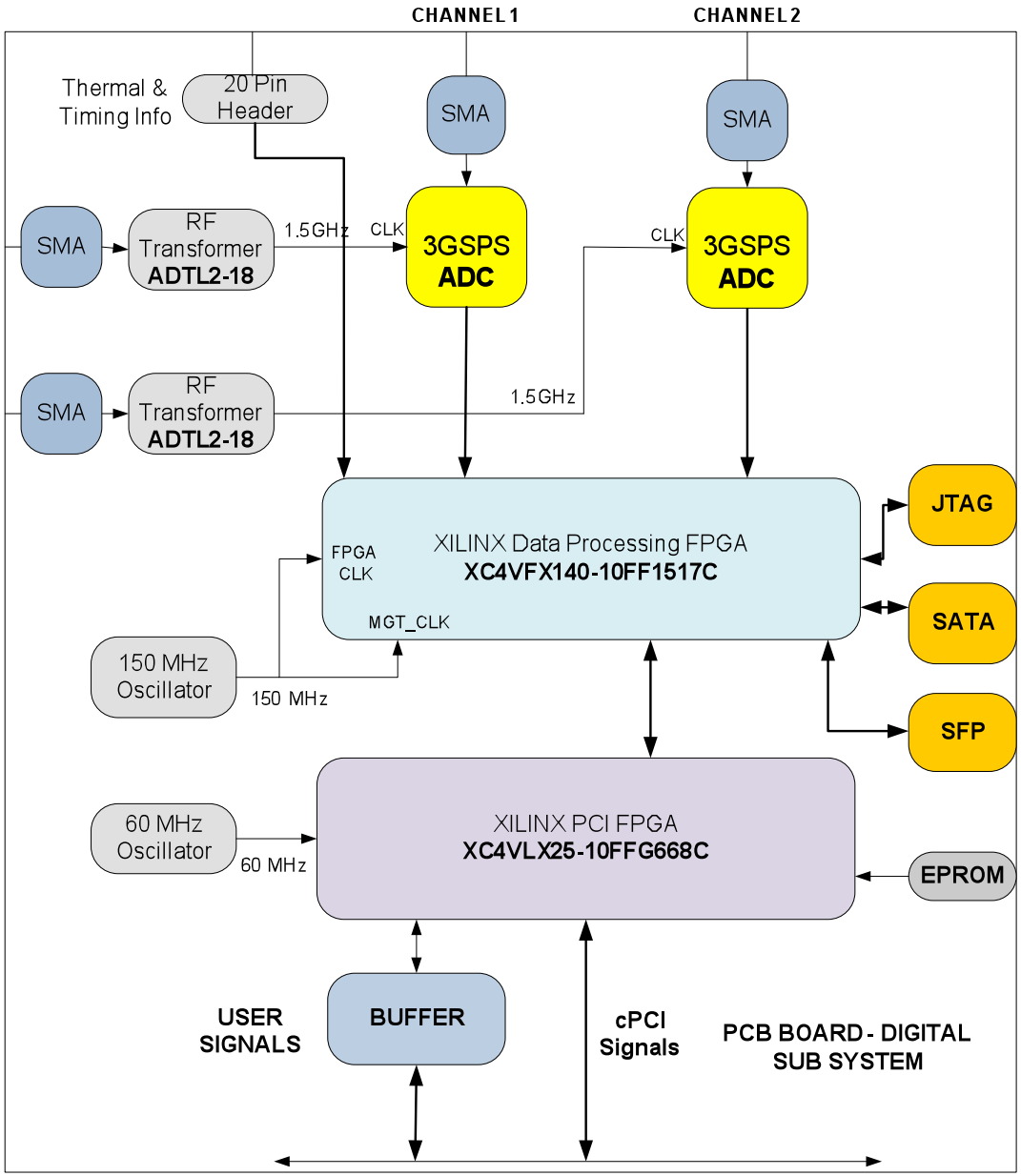
- Dynamic modeling of temperature is challenging because of the complexity of the subject matter
- Absolute accuracy is less important than the ability to capture the low order derivatives
- As modeling improves, we will incorporate the results into the observed phase behavior between the two channels
- Similar model results have been obtained using COMSOL. An emperical model is used currently for tuning the COMSOL model.
- Results will be used to better inform the microwave engineering

Thermal Analysis Wrapup

- We are pushing the technology of combining millemeterwave engineering with thermal analysis, to make the system more robust, balanced, and predictable
- Analysis will inform better design and post-processing methods of adjusting for thermal transitions
- Results will allow for better use of limited satellite resources (i.e. percentage of usable orbit)

Next: A High Performance Data Acquisition System

Data acquisition system

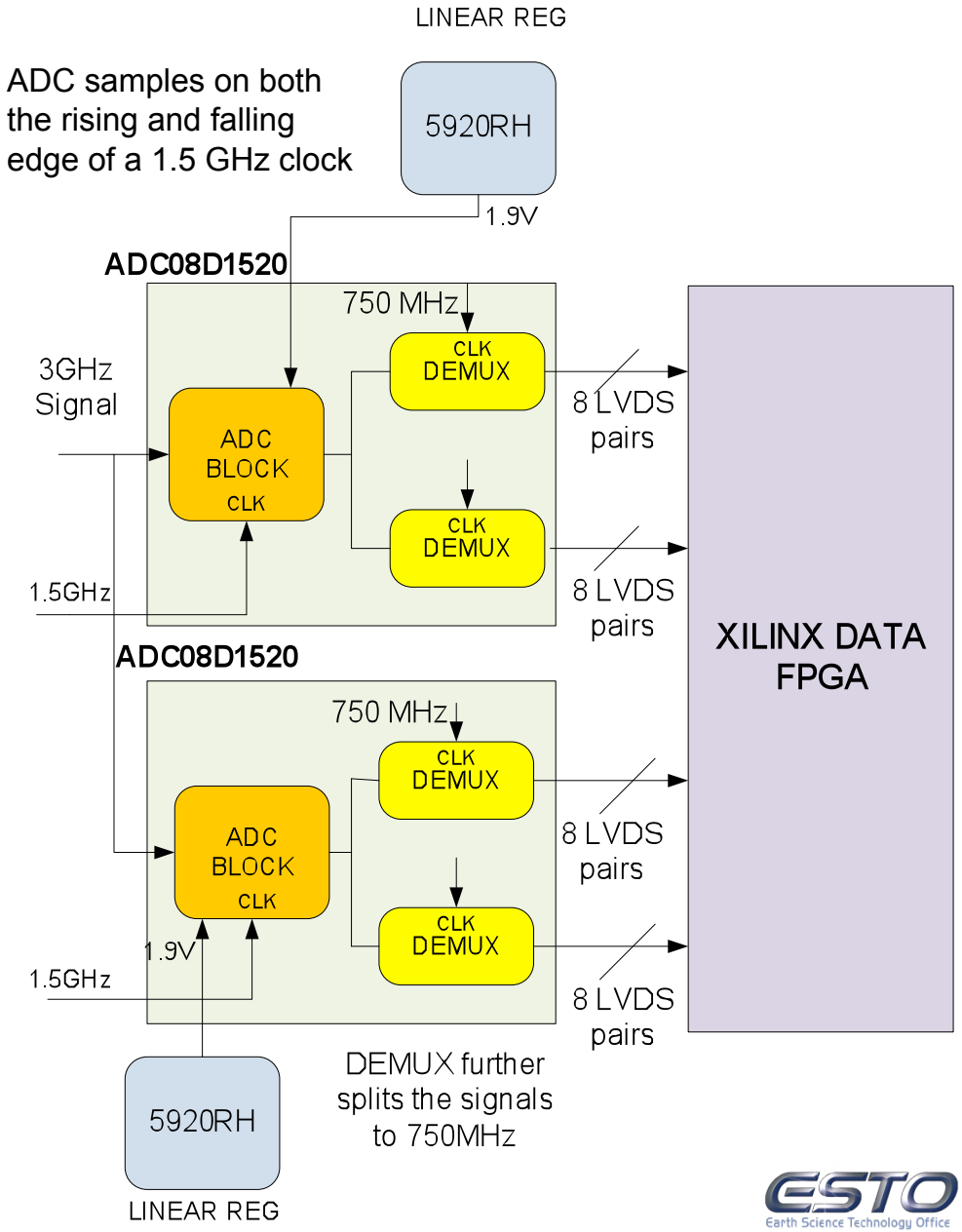


- The digital system is based on two 3GSamp/Sec ADC's from National Semiconductor, and two XILINX Virtex-4 FPGA's.

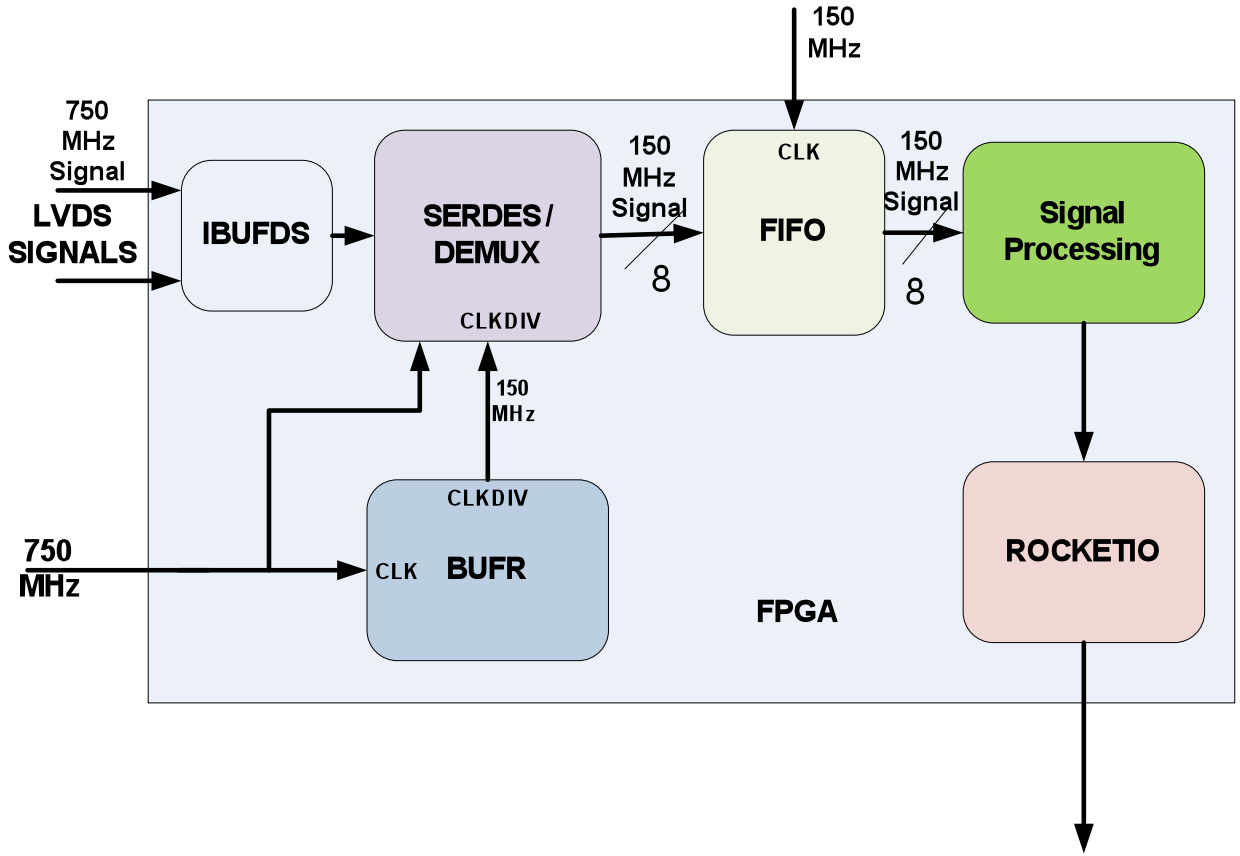
- All components, including voltage regulators, have space qualified equivalents.

- The "breadboard" system has multiple standard interfaces for programming and debugging. These may be easily removed from the design.

ADC ->Data FPGA Interfaces



DATA FPGA BLOCKS



IBUFDS - LVDS input buffer
SERDES - Serializer Deserializer/ Serial to Parallel converter
BUFR - Primitive clock buffer for IC
ROCKETIO - Multi Giga-bit transceiver
FIFO - First In First Out Queue

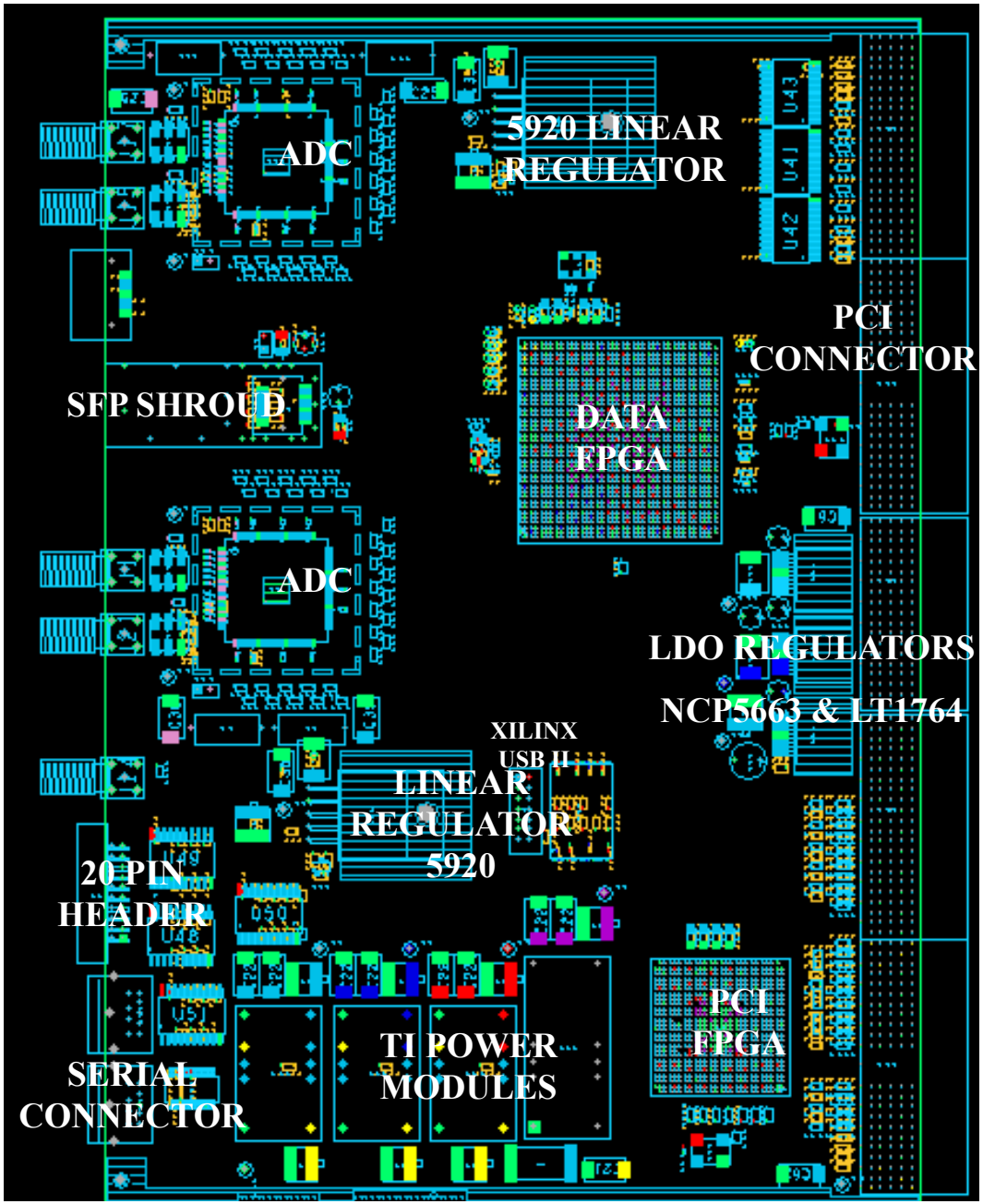
Board Layout

160 mm x 230 mm

14 layers

ports for SMA trigger, 20 pin header, 9 pin header, SFP and SATA Rocket I/O

Standard 6U PCI form factor



Design Considerations

- Decoupling capacitors for the FPGAs
  - One cap per every power pin
  - The proportion of high-frequency capacitors to low-frequency capacitors is an important factor
  - Low and flat power supply impedance from the 500KHz to 500 MHz range
- Space qualified counterparts for all components
- Two RocketIO interfaces allow for Gbit/s transfer
- FPGA and associated interfaces designed to run at 150 MHz
- PCI bus runs at 66 MHz

Design Considerations

- Differential pair termination
  - External 100 ohm resistors
  - Generally there are internal termination resistors on LVDS lines of Xilinx FPGA
  - These internal termination resistors on the Data FPGA are not used.
- Flexible clocking
  - SMA connectors for external signals
  - On-board oscillators
- The two ADCs are separately powered by 1.9V output linear regulators

BOM Major Parts

Sl. NO	Part	Part Number	Manufacturer
1	Data FPGA	XC4VFX140-10FFG1517C-ND	Xilinx
2	PCI FPGA	XC4VLX25 - 10FFG668C	Xilinx
3	Linear Regulators for ADCs	5920RH	MS Kennedy Corporation
4	Regulators for FPGAs	PTH 05010 - 1.2V	Texas Instruments
		PTH05060W - 1.8V, 3.3V, 2.5V	Texas Instruments
5	ADC	ADC08D1520	National Semiconductor
6	POWER SPLITTER	GP2S1+	Mini Circuits
7	BALUN	ADTL2-18	Mini Circuits

- Linear regulators have rad hard equivalents
- Other components are standard
- FPGAs have been donated by Xilinx, ADC by National Semiconductor, and Regulators by MS Kennedy

Power Estimate – DATA FPGA Logic Resources Utilization

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.61177 (W)	5	---	---
Logic	0.00038 (W)	104	126336	0.1
Signals	0.00189 (W)	411	---	---
IOs	1.08536 (W)	280	876	32.0
DCMs	0.00000 (W)	0	20	0.0
MGTs	0.57084 (W)	2	24	8.3
Total Quiescent Power	**1.83274 (W)**			
Total Dynamic Power	**2.25719 (W)**			
Total Power	**4.08994 (W)**			

Power Analysis

- Xilinx ISE tool set provides a power analysis feature
- The tool estimates static and dynamic power
  - Random inputs assumed
  - Averaged over time period
  - Power estimate of 2 FPGAs = 8W
- Total Power estimate of the board
  - ADCs power consumption = 4W
  - Other components = 1W
  - Total = 13W

Advancing the TRL